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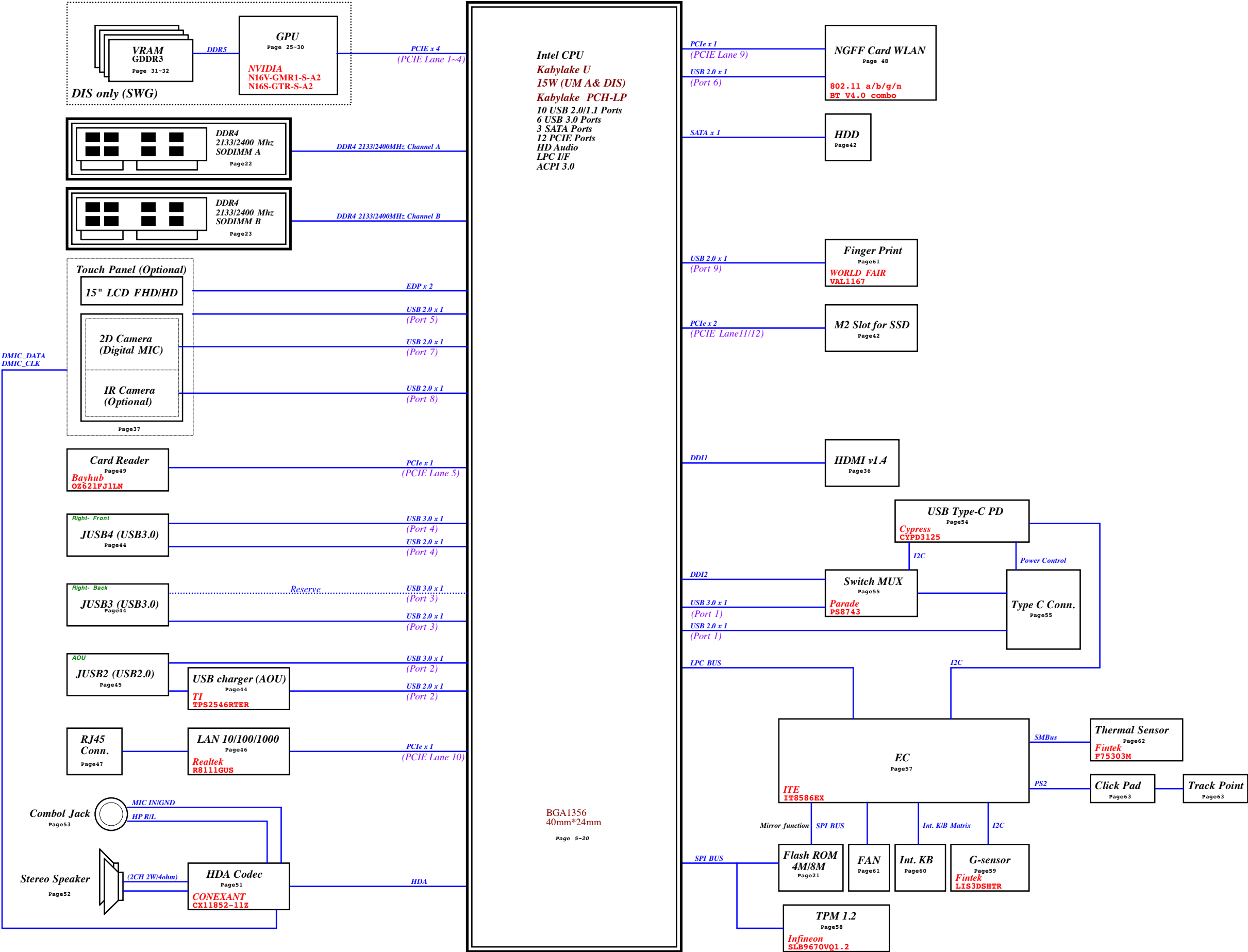
KENOBI NM-A821 Rev2.0 Schematic

Intel KabyLake Processor with DDR4 + PCH-LP

NVIDIA N16V-GMR GDDR3 2GB

2016-08-24 Rev2.0

Kenobi KBL U Block Diagram



Voltage Rails (O --> Means ON , X --> Means OFF)

<div>Power Plane</div> <div>State</div>	B+ +3VL	+3VALW +5VALW +1VALW +1.8VALW	+2.5V +1.2V +VCC_STG	+5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VGA_CORE +3VS_VGA +1.5VS_VGA +3VS_AON +1VS_VGA +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#	SYSON
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	HIGH
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF	LOW
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF	LOW

SMBUS Control Table

	SOURCE	Main VGA	BATT (Charger)	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	LAN PHY	G sensor	USB Type-C
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580F +3VL	X	X	X	X	X	X	X	X	X	V +3VPD_VDD
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	V +3VS_GS	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	X	X	X	V +5VS	X	X	X
PCH_SML1CLK PCH_SML1DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	X	X

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
XDP@	Debug port
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
SSD@	SSD setting
FRP@	Finger printer setting
TYPEC@	For USB Type-C function
ME@	ME Connector
EMC@	For EMC function
EMC_2D@	For EMC function
EMC_NS@	For EMC function
RF_NS@	For RF function
S2G@	For VRAM Strap
CHA@	For VRAMA function
CHB@	For VRAMB function
RANKA@	GPU DDR5 Setting
X76@	GPU VRAM Setting
3DCCD@	3D Camera Setting
VGA@	VGA Setting
MUX@	MUX Setting
ODD@	ODD Setting
TPM@	Trusted Platform Module (TPM)
MIRROR@	For mirror function
NGC6@	For VGA Non GC6 function
GC6@	For VGA GC6 function

USB2 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	JUSB3
4	JUSB4
5	Touch Panel
6	BT
7	CMOS
8	IR CAMERA
9	FP/Smart

USB3 Port

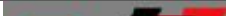
Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	JUSB3
4	JUSB4

PCIE Port

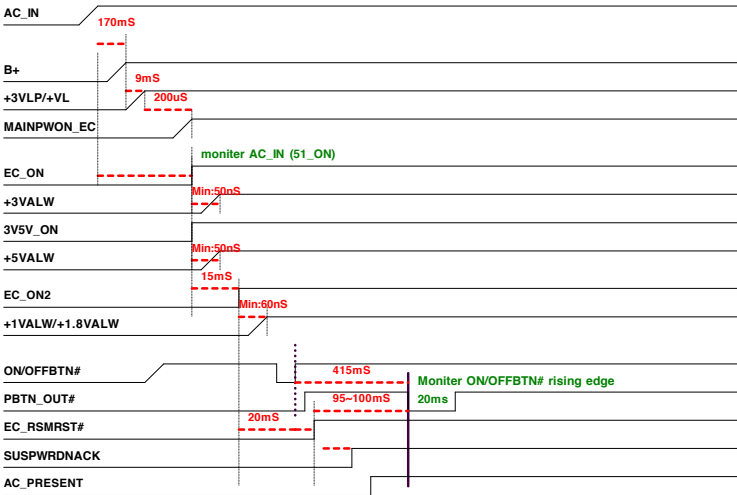
Port	Device
1	GPU
2	GPU
3	GPU
4	GPU
5	CardReader
6	X
7	X
8	X
9	WLAN
10	LAN
11	M.2 SSD
12	M.2 SSD

SATA Port

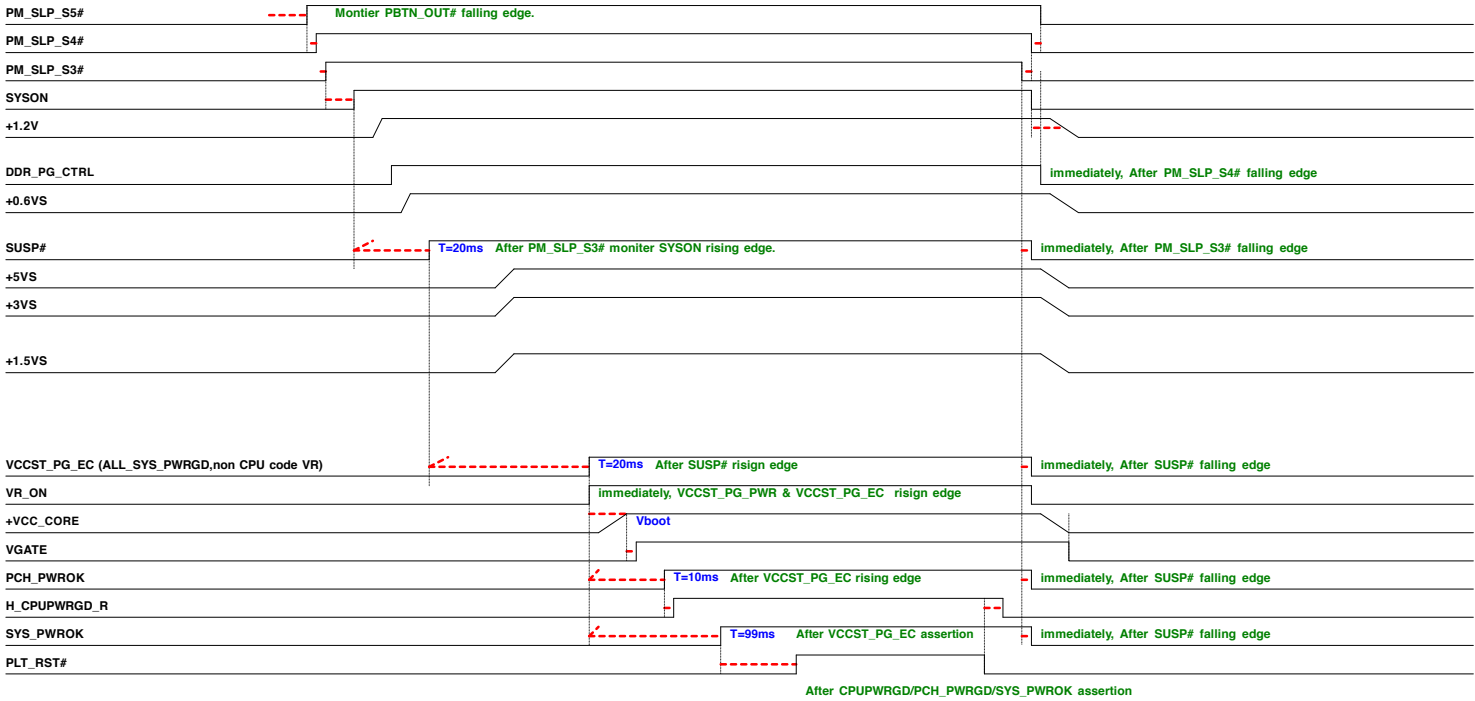
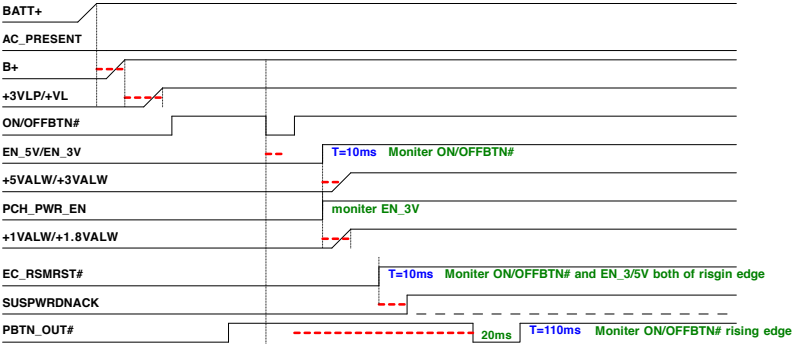
Port	Device
1	HDD
2	X
3	X
4	X

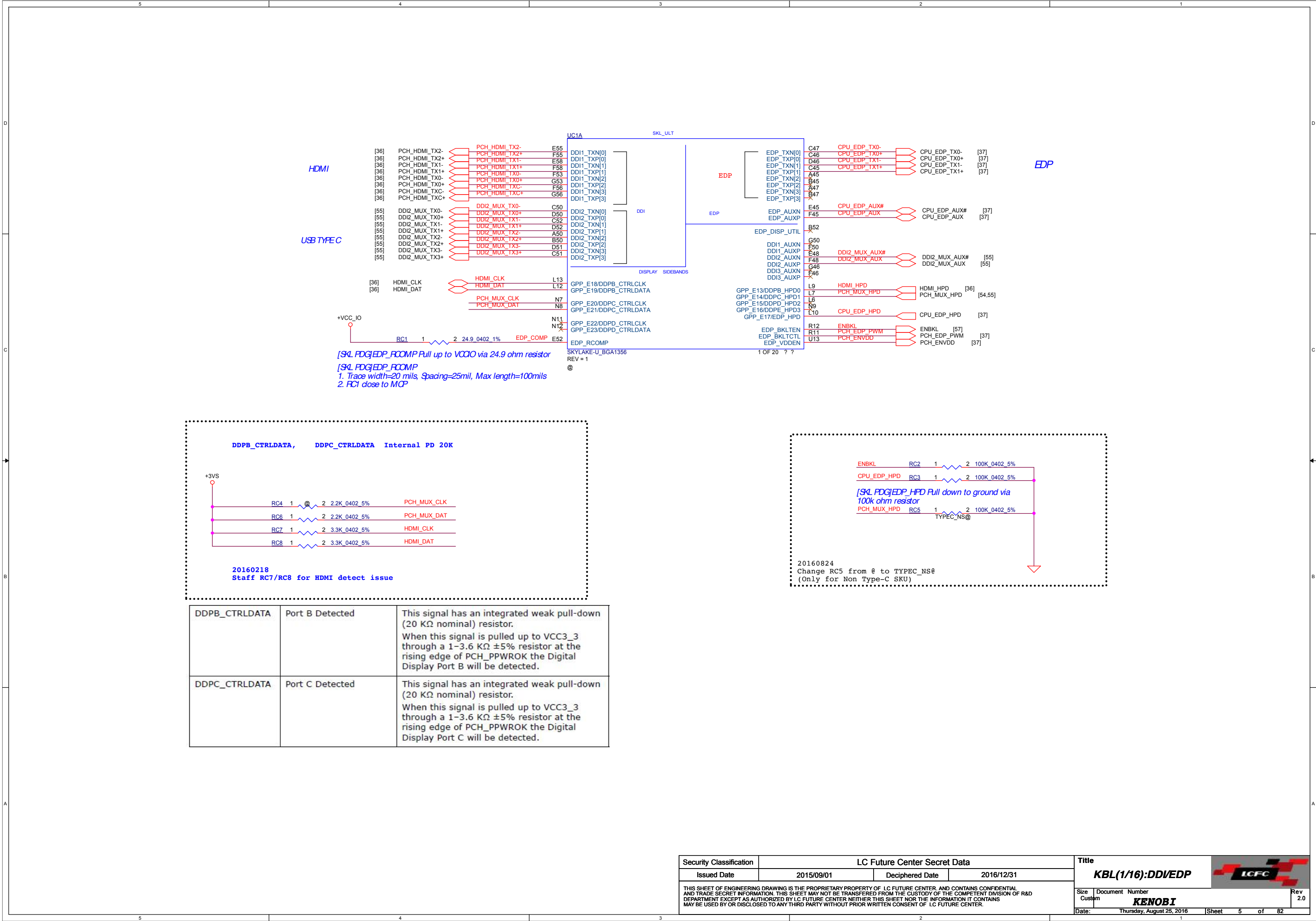
Security Classification		LC Future Center Secret Data		Title		
Issued Date		2015/10/5	Deciphered Date	2016/12/31	NOTE LIST	
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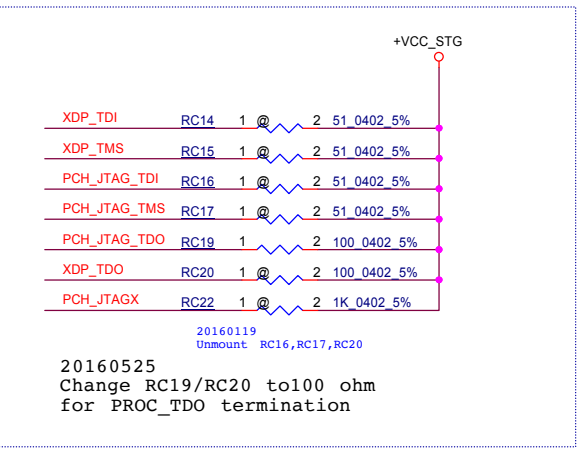
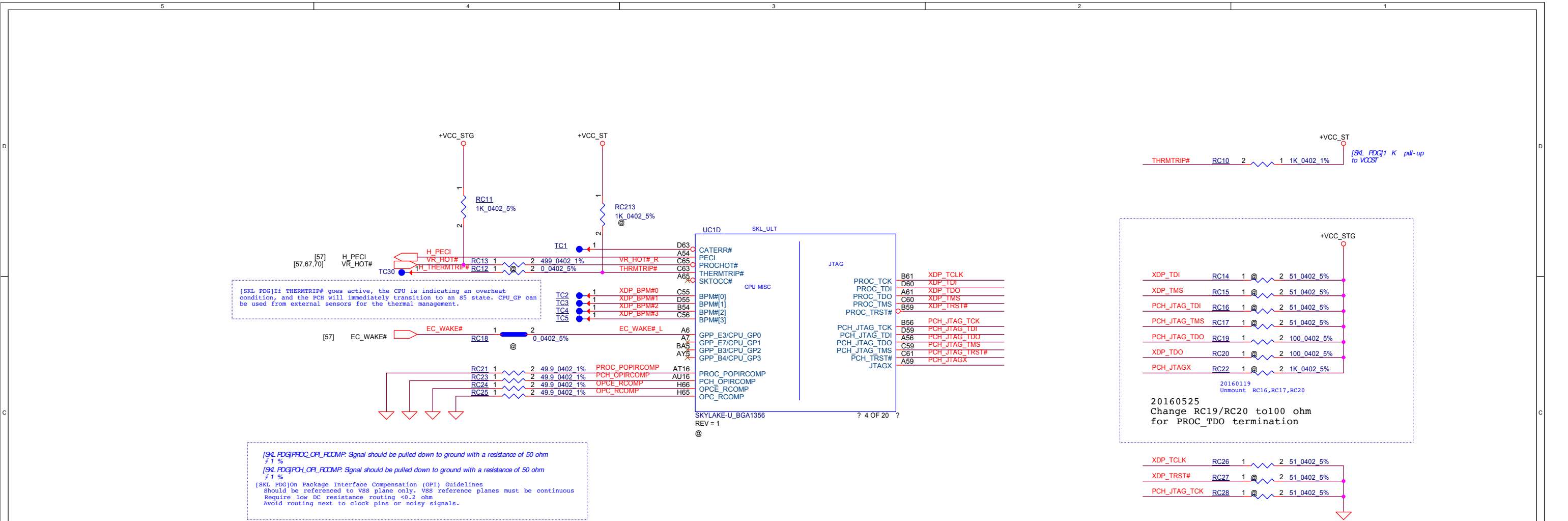
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[DC Mode]

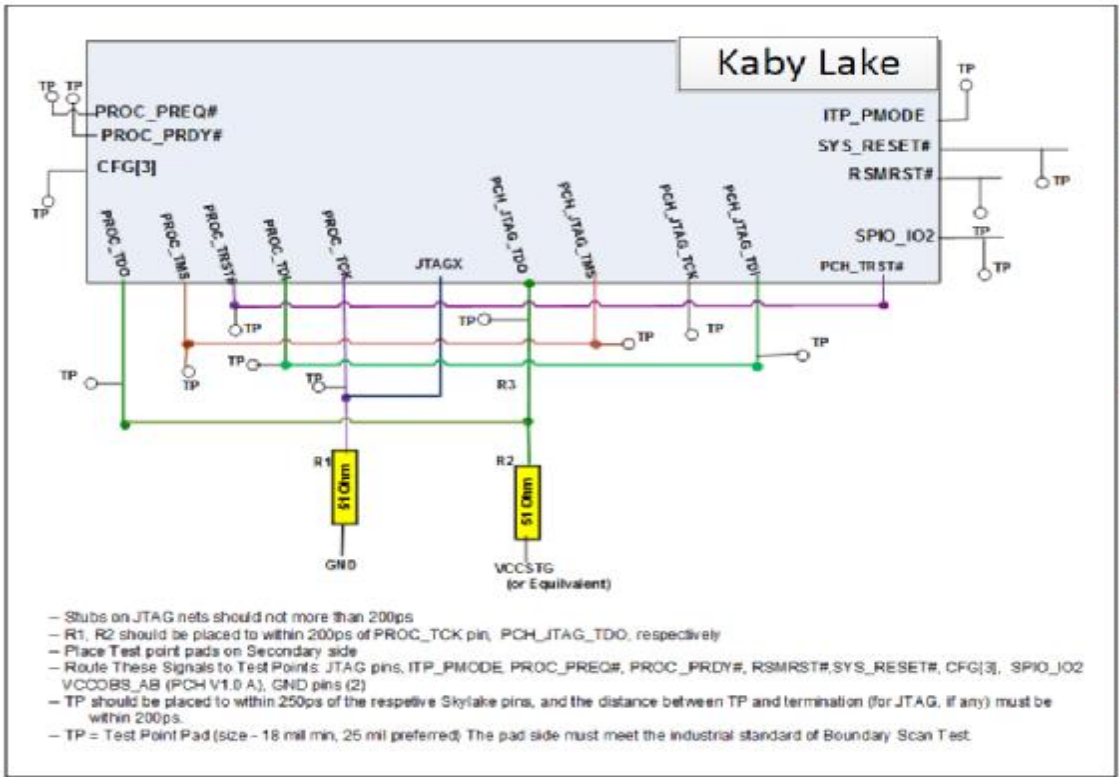






Termination option

XDP_TCLK PROC_TCK Termination: 51 ohm +/- 5% pull down to GNG (Ground) Placed to within 200ps (1100 mil) or PROC_TCK pin
PCH_JTAG_TDO PCH_JTAG_TDO Termination: 51ohm +/- 5% pull up to VccSTG or equivalent. Placed to within 200ps (1100 mil) or PCH_JTAG_TDO pin



XDP_TCLK	RC29	1	DCI@	2	0	0402	5%	PCH_JTAGX
XDP_TDI	RC30	1	DCI@	2	0	0402	5%	PCH_JTAG_TDI
XDP_TDO	RC31	1	DCI@	2	0	0402	5%	PCH_JTAG_TDO
XDP_TMS	RC32	1	DCI@	2	0	0402	5%	PCH_JTAG_TMS
XDP_TRST#	RC33	1	DCI@	2	0	0402	5%	PCH_JTAG_TRST#

Close to UC1

TABLE			
	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL88	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL89	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR88	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU88	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR89	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU89	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB66	DDR0_DQ[16]	DDR0_DQ[32]
	AW66	DDR0_DQ[17]	DDR0_DQ[33]
	AW69	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA66	DDR0_DQ[20]	DDR0_DQ[36]
	AY66	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB69	DDR0_DQ[26]	DDR0_DQ[42]
	AW69	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA69	DDR0_DQ[30]	DDR0_DQ[46]
	AY69	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY36	DDR0_DQ[40]	DDR1_DQ[8]
	AW36	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB36	DDR0_DQ[44]	DDR1_DQ[12]
	BA36	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 8	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	AY29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY26	DDR0_DQ[58]	DDR1_DQ[42]
	AW26	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA26	DDR0_DQ[62]	DDR1_DQ[46]
	BB26	DDR0_DQ[63]	DDR1_DQ[47]

TABLE			
	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

TABLE			
Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[3]	DDR0_CAA[1]	DDR0_MA[3]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BA[2]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[9]	DDR0_CAB[9]	DDR0_MA[9]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

[22] DDR_A_D[63..0]

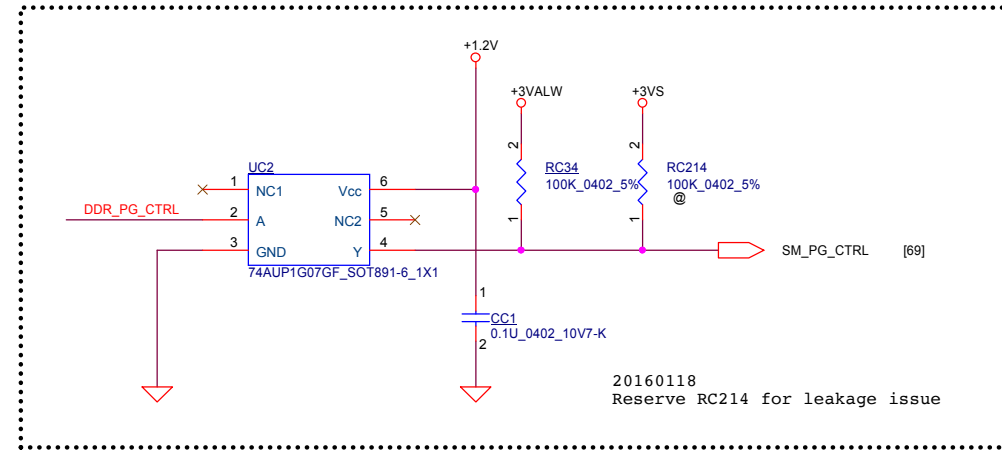


TABLE			
	Pin	Interleave	Non-Interleave
Block 1	AF86	DDR1_DQ[0]	DDR0_DQ[16]
	AF84	DDR1_DQ[1]	DDR0_DQ[17]
	AK86	DDR1_DQ[2]	DDR0_DQ[18]
	AK84	DDR1_DQ[3]	DDR0_DQ[19]
	AF88	DDR1_DQ[4]	DDR0_DQ[20]
	AF87	DDR1_DQ[5]	DDR0_DQ[21]
	AK87	DDR1_DQ[6]	DDR0_DQ[22]
	AK88	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF88	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH88	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF88	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH88	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT88	DDR1_DQ[16]	DDR0_DQ[48]
	AU88	DDR1_DQ[17]	DDR0_DQ[49]
	AP86	DDR1_DQ[18]	DDR0_DQ[50]
	AN86	DDR1_DQ[19]	DDR0_DQ[51]
	AP88	DDR1_DQ[20]	DDR0_DQ[52]
	AT86	DDR1_DQ[21]	DDR0_DQ[53]
	AU86	DDR1_DQ[22]	DDR0_DQ[54]
	AU88	DDR1_DQ[23]	DDR0_DQ[55]
	AT81	DDR1_DQ[24]	DDR0_DQ[56]
	AU81	DDR1_DQ[25]	DDR0_DQ[57]
	AP80	DDR1_DQ[26]	DDR0_DQ[58]
	AN80	DDR1_DQ[27]	DDR0_DQ[59]
	AN81	DDR1_DQ[28]	DDR0_DQ[60]
	AP81	DDR1_DQ[29]	DDR0_DQ[61]
	AT80	DDR1_DQ[30]	DDR0_DQ[62]
	AU80	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT26	DDR1_DQ[50]	DDR1_DQ[50]
	AU26	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN26	DDR1_DQ[54]	DDR1_DQ[54]
	AP26	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

TABLE			
	Pin	Interleave	Non-Interleave
Block 1	AH86	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE			
Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_GAA[0]	DDR1_MA[5]
AP90	DDR1_MA[8]	DDR1_GAA[1]	DDR1_MA[8]
BA48	DDR1_MA[6]	DDR1_GAA[2]	DDR1_MA[6]
BS48	DDR1_MA[8]	DDR1_GAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_GAA[4]	DDR1_MA[7]
AP82	DDR1_BA[2]	DDR1_GAA[5]	DDR1_BA[2]
AN50	DDR1_MA[12]	DDR1_GAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_GAA[7]	DDR1_MA[11]
AN53	DDR1_MA[10]	DDR1_GAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_GAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[16]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BS44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[11]	DDR1_CAB[8]	DDR1_MA[11]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

[23] DDR_B_D[0..63]

UC1C

SKL_ULT

DDR_B_D0 AF65
DDR_B_D1 AF64
DDR_B_D2 AK65
DDR_B_D3 AK64
DDR_B_D4 AF66
DDR_B_D5 AF67
DDR_B_D6 AK67
DDR_B_D7 AK66
DDR_B_D8 AF70
DDR_B_D9 AF68
DDR_B_D10 AH71
DDR_B_D11 AH68
DDR_B_D12 AF71
DDR_B_D13 AF69
DDR_B_D14 AH70
DDR_B_D15 AH69
DDR_B_D16 AT68
DDR_B_D17 AU68
DDR_B_D18 AP65
DDR_B_D19 AN65
DDR_B_D20 AN66
DDR_B_D21 AP66
DDR_B_D22 AT65
DDR_B_D23 AU65
DDR_B_D24 AU61
DDR_B_D25 AP60
DDR_B_D26 AN60
DDR_B_D27 AN61
DDR_B_D28 AN61
DDR_B_D29 AP61
DDR_B_D30 AT60
DDR_B_D31 AU60
DDR_B_D32 AU40
DDR_B_D33 AT40
DDR_B_D34 AT37
DDR_B_D35 AU37
DDR_B_D36 AR40
DDR_B_D37 AP40
DDR_B_D38 AP37
DDR_B_D39 AR37
DDR_B_D40 AT33
DDR_B_D41 AU33
DDR_B_D42 AU30
DDR_B_D43 AT30
DDR_B_D44 AR33
DDR_B_D45 AP33
DDR_B_D46 AR30
DDR_B_D47 AP30
DDR_B_D48 AU27
DDR_B_D49 AT27
DDR_B_D50 AT26
DDR_B_D51 AU26
DDR_B_D52 AP27
DDR_B_D53 AN27
DDR_B_D54 AN26
DDR_B_D55 AP26
DDR_B_D56 AT22
DDR_B_D57 AU22
DDR_B_D58 AU21
DDR_B_D59 AR21
DDR_B_D60 AN22
DDR_B_D61 AP21
DDR_B_D62 AP21
DDR_B_D63 AN21

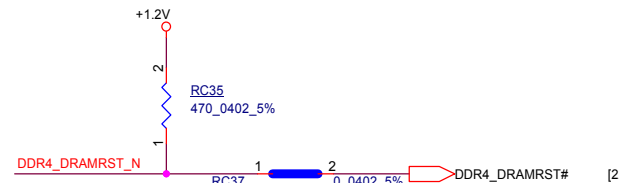
SKYLAKE-U_BGA1356
REV = 1
@


[KBL PDG] for DDR4 COMPENSATION
DDR_RCOMP[0] Pull down 121 ohm resistor
DDR_RCOMP[1] Pull down 80.6 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

DDR_B_MA0
DDR_B_MA1
DDR_B_MA2
DDR_B_MA3
DDR_B_MA4
DDR_B_MA5
DDR_B_MA6
DDR_B_MA7
DDR_B_MA8
DDR_B_MA9
DDR_B_MA10
DDR_B_MA11
DDR_B_MA12
DDR_B_MA13
DDR_B_MA14
DDR_B_MA15
DDR_B_MA16

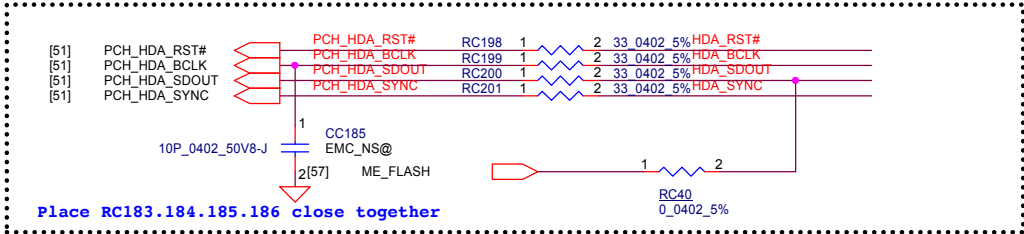
DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7

DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7

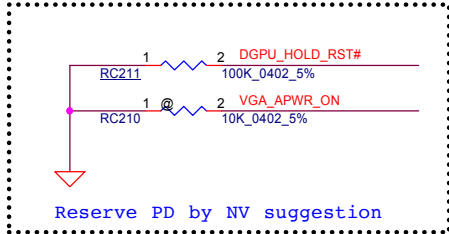
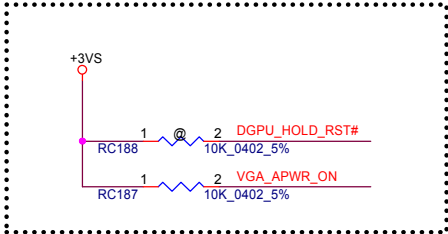


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Issued Date		2015/09/01		Deciphered Date		2016/12/31			
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Size		Document		Number		Rev			
Custom		KENOBI		2.0					
Date:				Thursday, August 25, 2016		Sheet		8 of 82	

[KBL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.

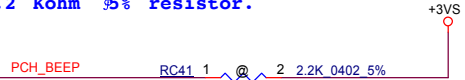


20160408
1.Unstaff RC188 and Staff RC211 with 100K resistor

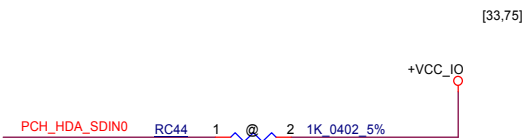


Note:
SPKR (PC_BEEP) has an integrated weak pull-down resistor (20 K ohm nominal) to disable Top-Block Swap by default.

To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 Kohm 5% resistor.



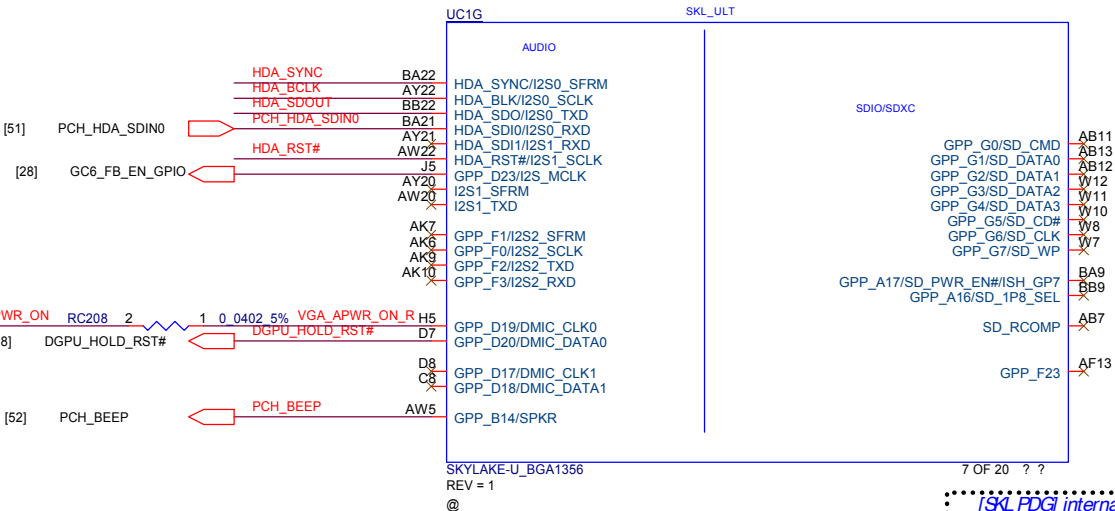
Note:
Internal PD 20K



Note:
HDA_SDO should only be asserted high via external pull-up to 3.3A rail in manufacturing/debug environments ONLY.



Note:
Internal PD 20K



[SKL PDG] internal SD Card

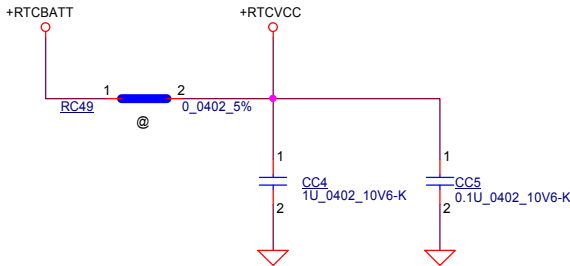
Not support internal SD card. Remove SD_RCOMP

Security Classification			
LC Future Center Secret Data			
Issued Date	2015/09/01	Deciphered Date	2016/12/31
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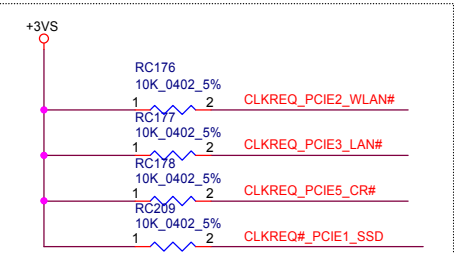
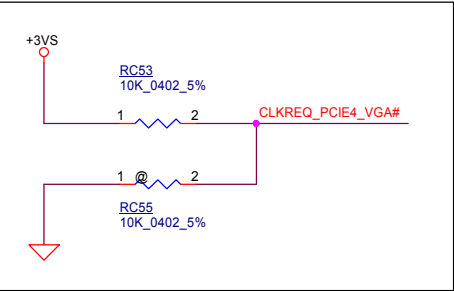
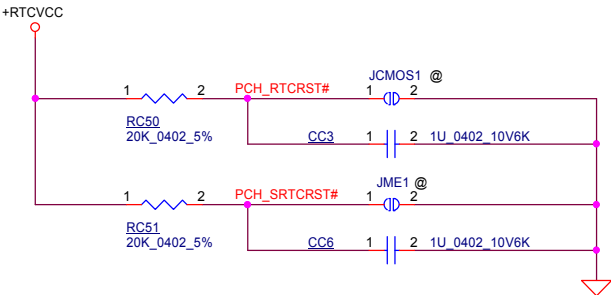
Title			
KBL(5/16):HDA/SDIO			
Size	Document	Number	Rev
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RTC External Circuit

+RTCBATT, +RTCVCC
Trace width = 20mils



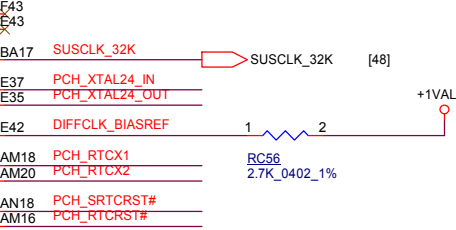
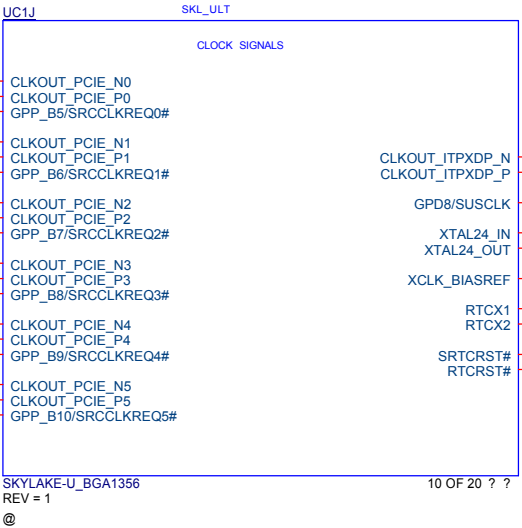
JCMOS, JME Setting, Need Under DDR Door



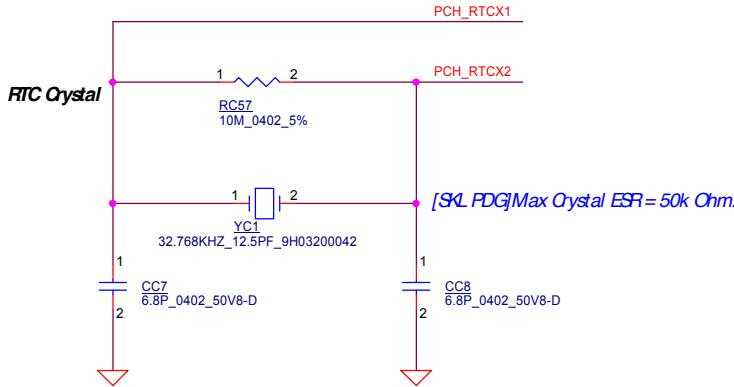
Place RC176,177,178,209 close together

M.2 SSD	[42]	CLK_PCIE_SSD#	CLK_PCIE_SSD#	B42
	[42]	CLK_PCIE_SSD	CLK_PCIE_SSD	A42
	[42]	CLKREQ#_PCIE1_SSD	CLKREQ#_PCIE1_SSD	A17
WLAN	[48]	CLK_PCIE_WLAN#	CLK_PCIE_WLAN#	D41
	[48]	CLK_PCIE_WLAN	CLK_PCIE_WLAN	C41
	[48]	CLKREQ#_PCIE2_WLAN#	CLKREQ#_PCIE2_WLAN#	A18
LAN	[46]	CLK_PCIE_LAN#	CLK_PCIE_LAN#	D40
	[46]	CLK_PCIE_LAN	CLK_PCIE_LAN	C40
	[46]	CLKREQ#_PCIE3_LAN#	CLKREQ#_PCIE3_LAN#	A10
VGA	[25]	CLK_PCIE_VGA#	CLK_PCIE_VGA#	B40
	[25]	CLK_PCIE_VGA	CLK_PCIE_VGA	A40
	[25]	CLKREQ#_PCIE4_VGA#	CLKREQ#_PCIE4_VGA#	A08
CR	[49]	CLK_PCIE_CR#	CLK_PCIE_CR#	E40
	[49]	CLK_PCIE_CR	CLK_PCIE_CR	E38
	[49]	CLKREQ#_PCIE5_CR#	CLKREQ#_PCIE5_CR#	A07

[SKL PDG]External pull-up resistor required if used for CLKREQ# functionality.

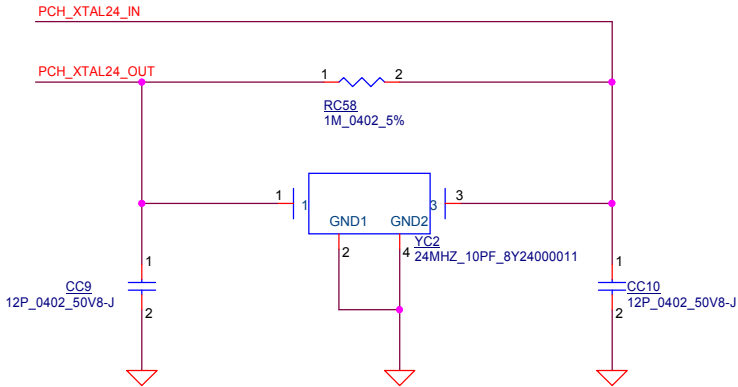


[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on opposit side of MCP for temp influence
4.The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations
Typical values for C1 and C2 are 18 pF based on crystal load of 12.5 pF.

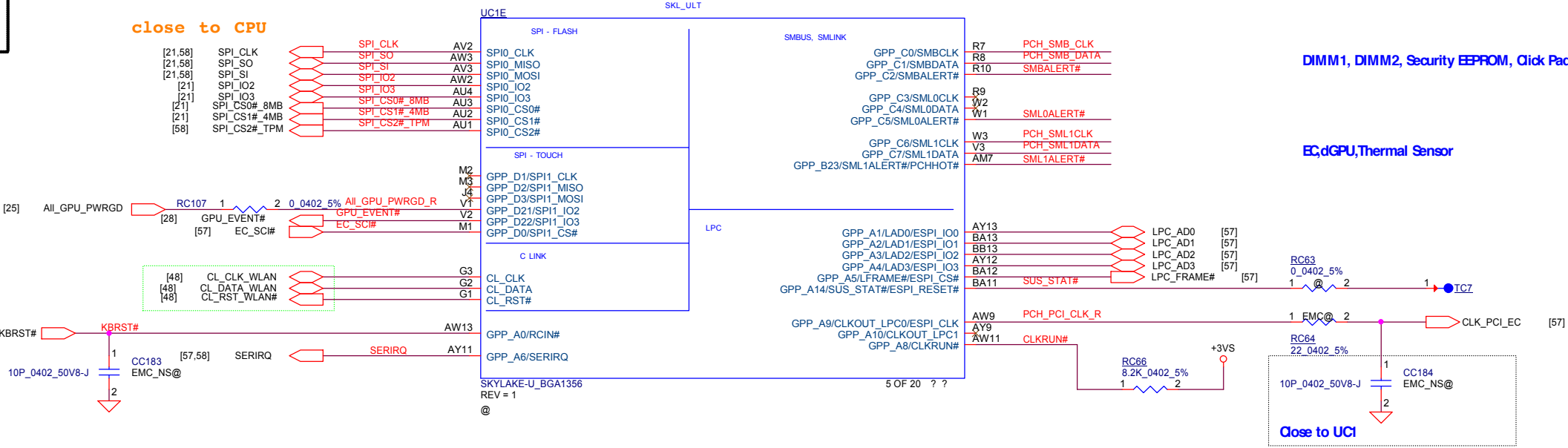
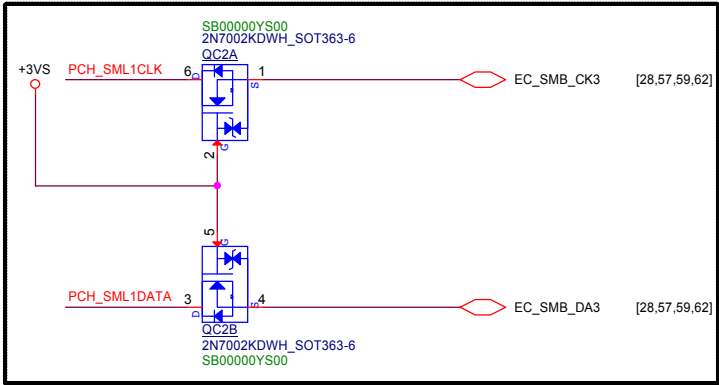
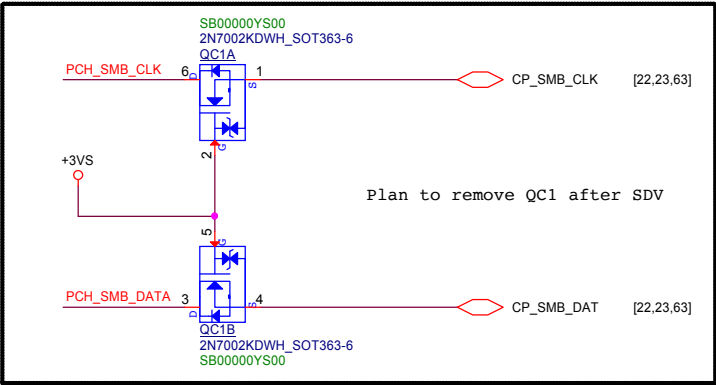
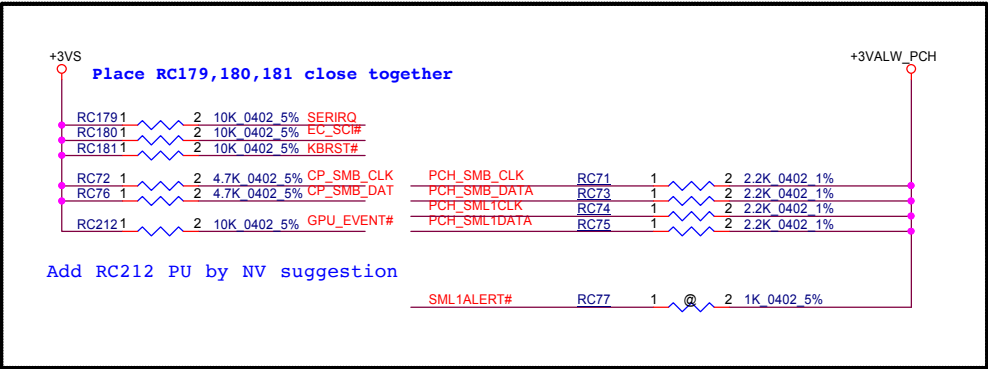
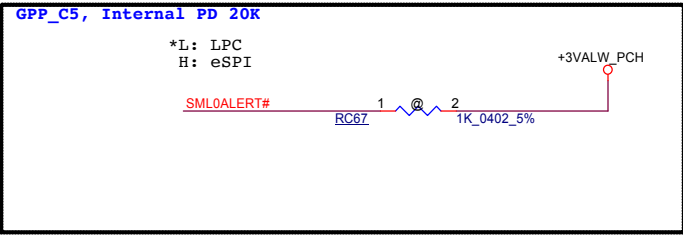
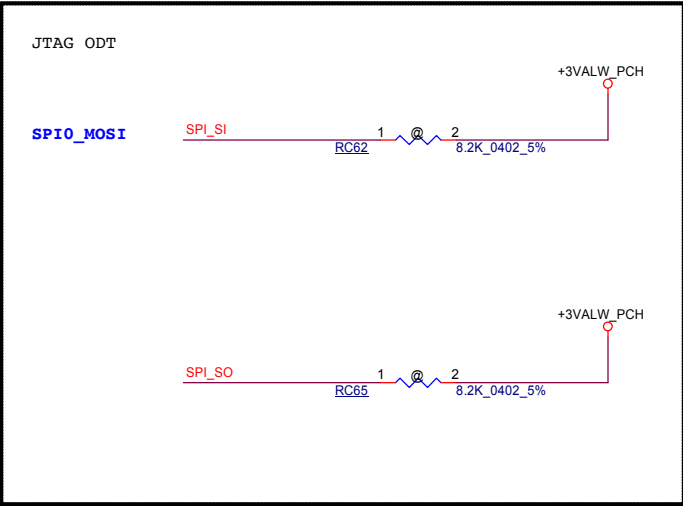
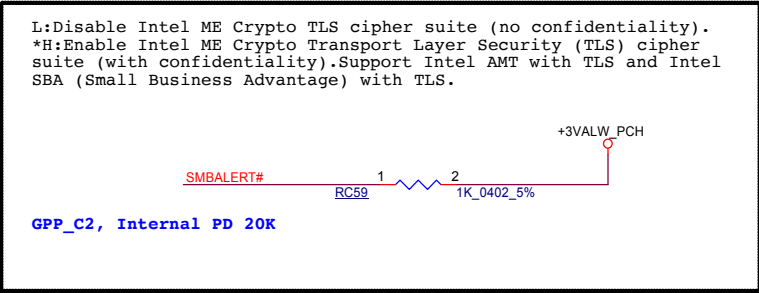


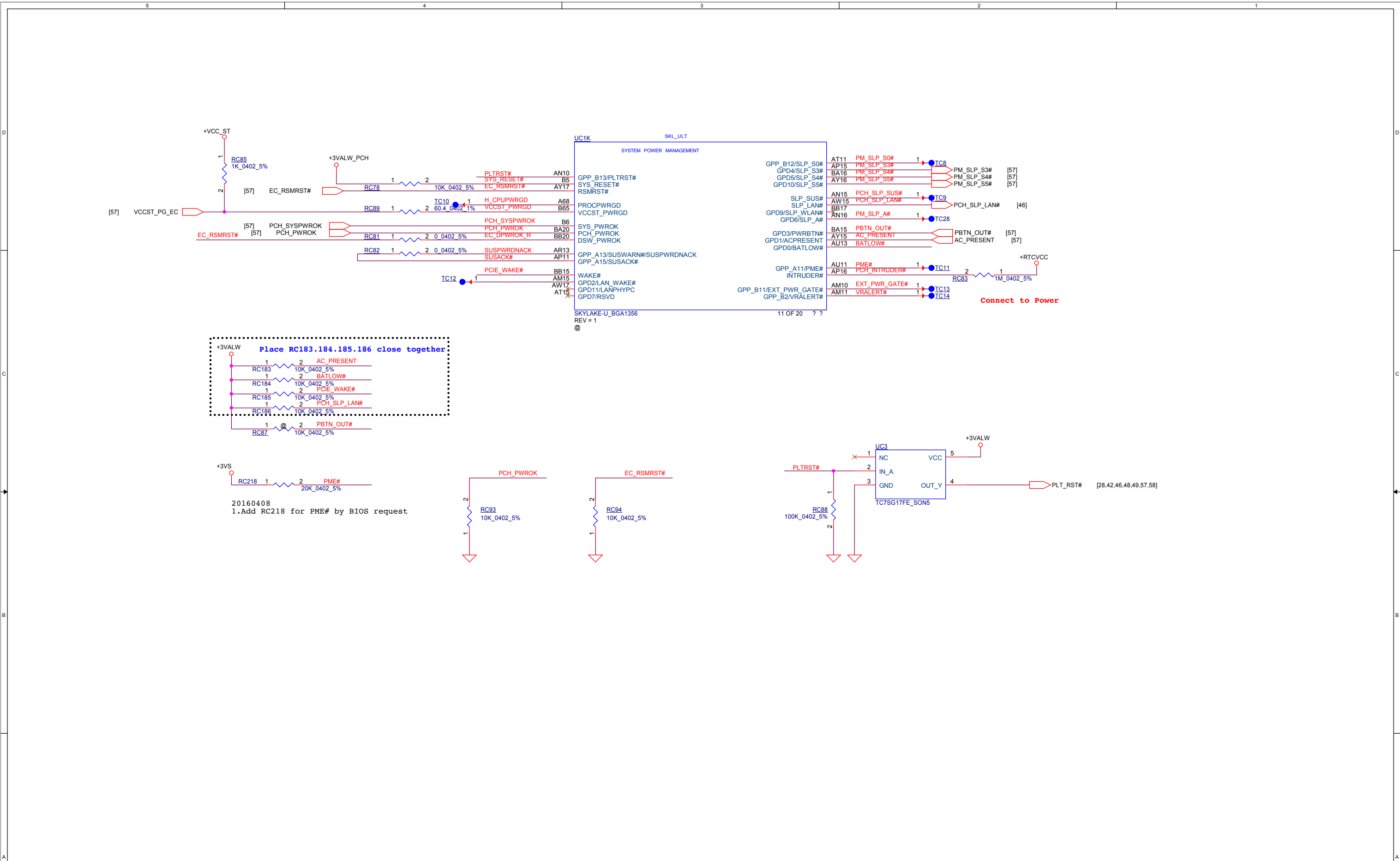
20160127
Change CC7/CC8 to 6.8p by vender suggestion

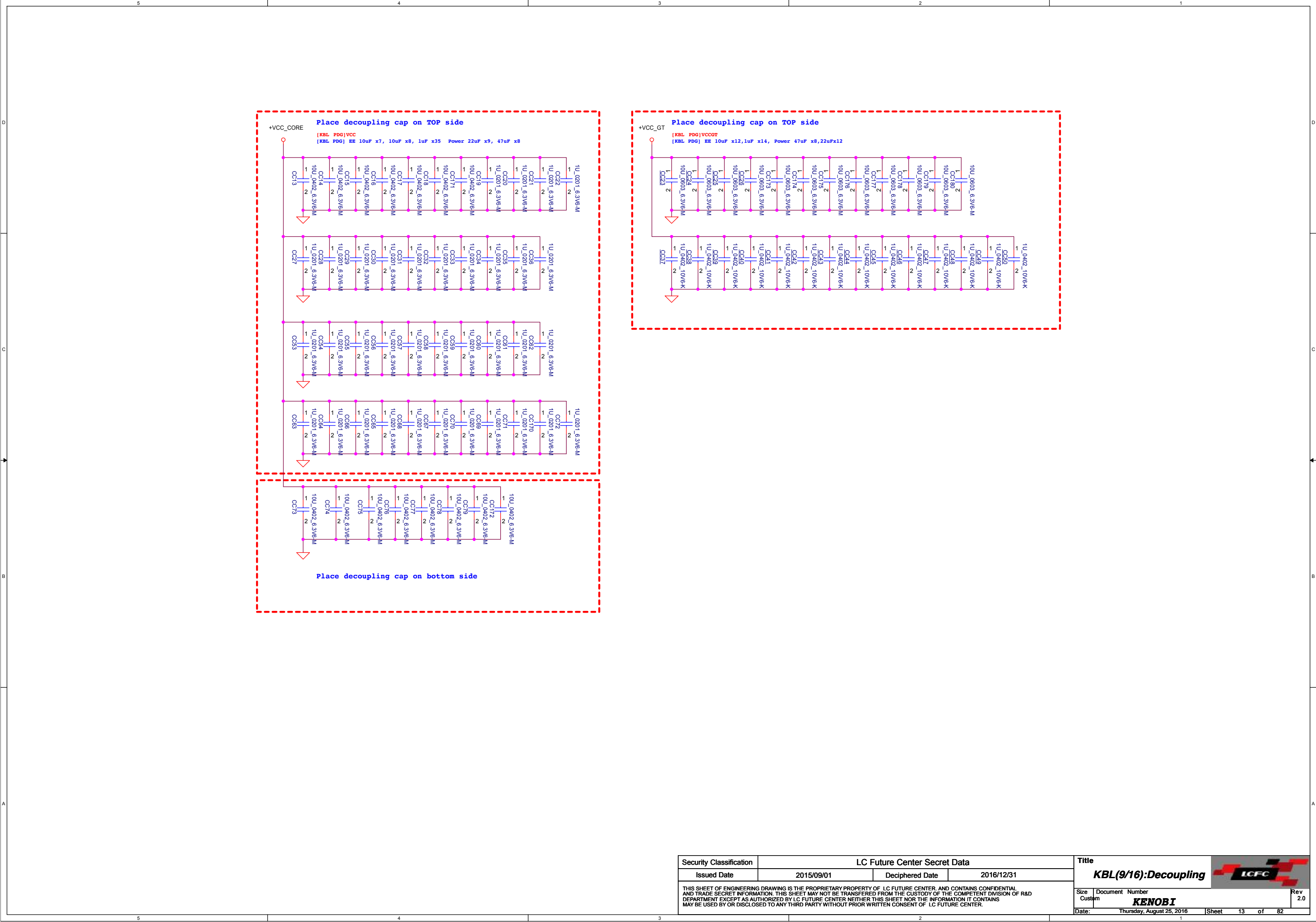
[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (C1 and C2)
3.A 1-Mohm bias resistor (R1)



Functional Strap Definitions



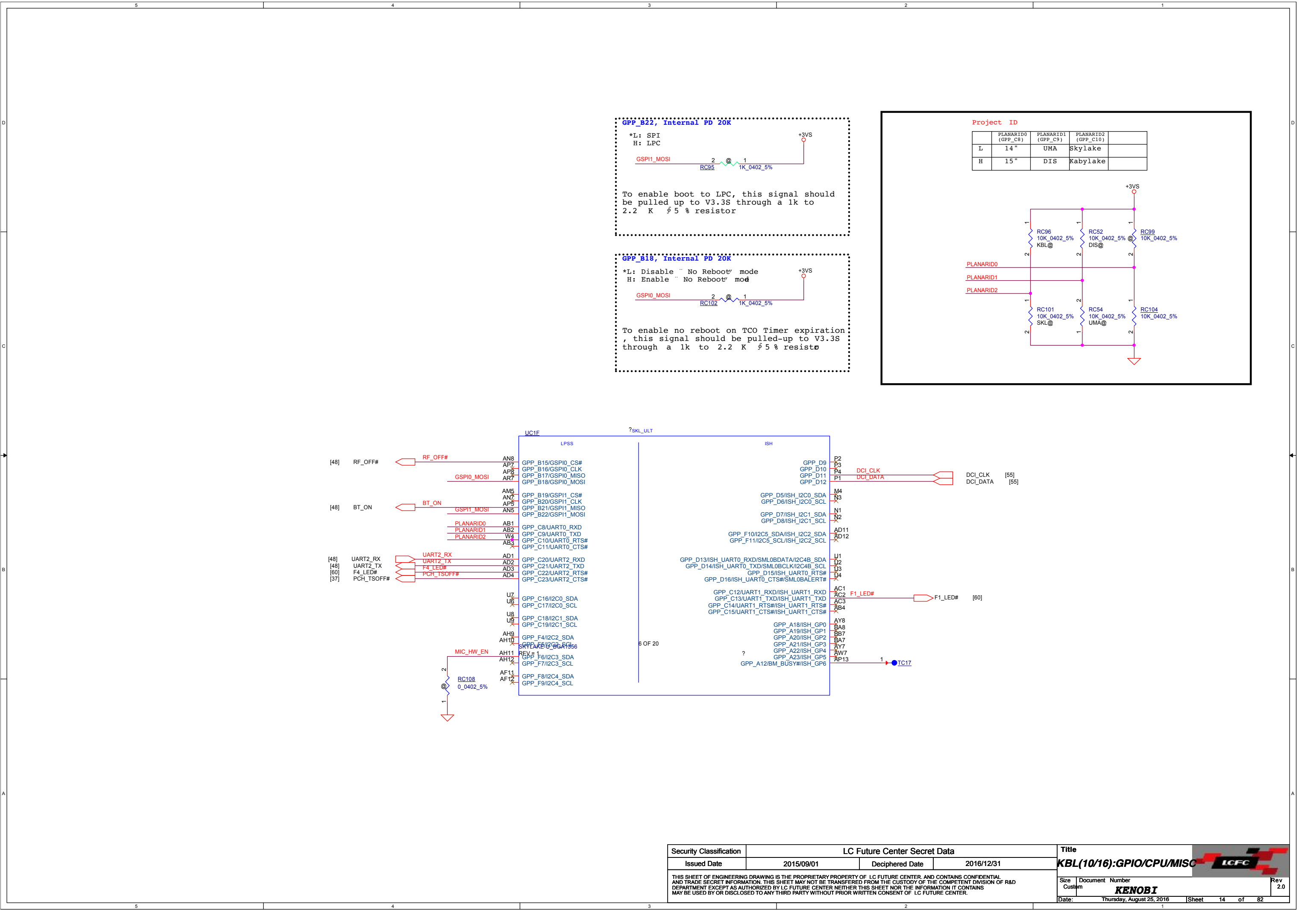


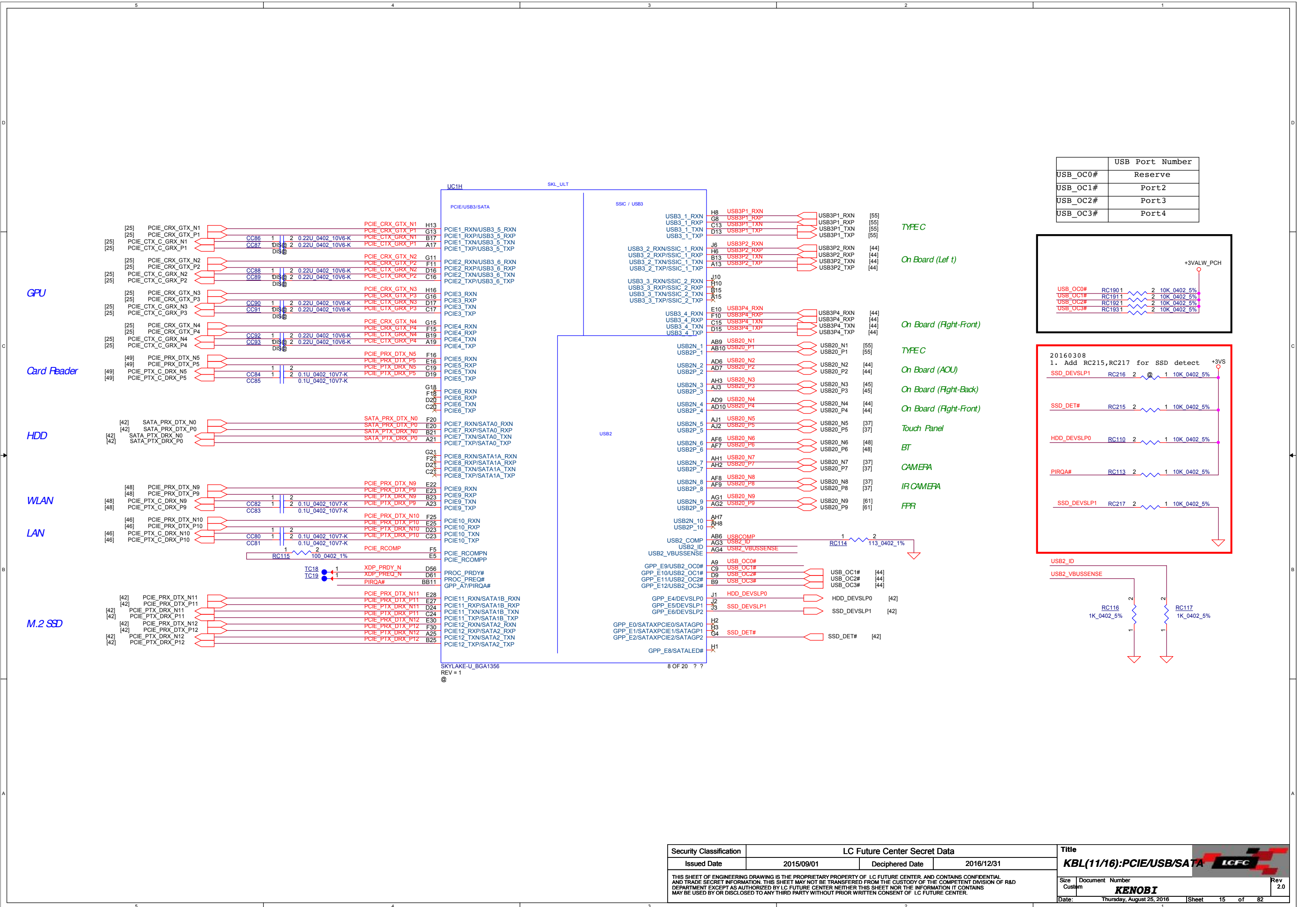


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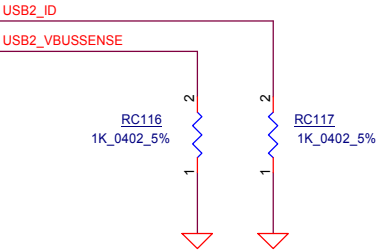
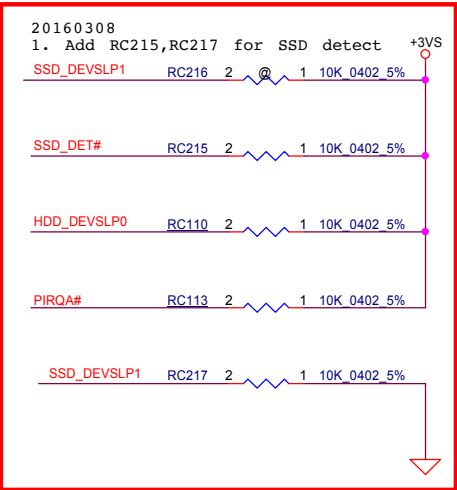
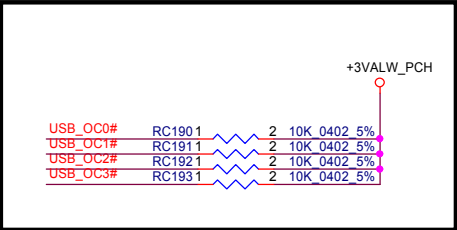
Title		KBL(9/16):Decoupling	
Size	Document	Number	Rev
Custom		KENOBI	2.0
Date:	Thursday, August 25, 2016	Sheet	13 of 82

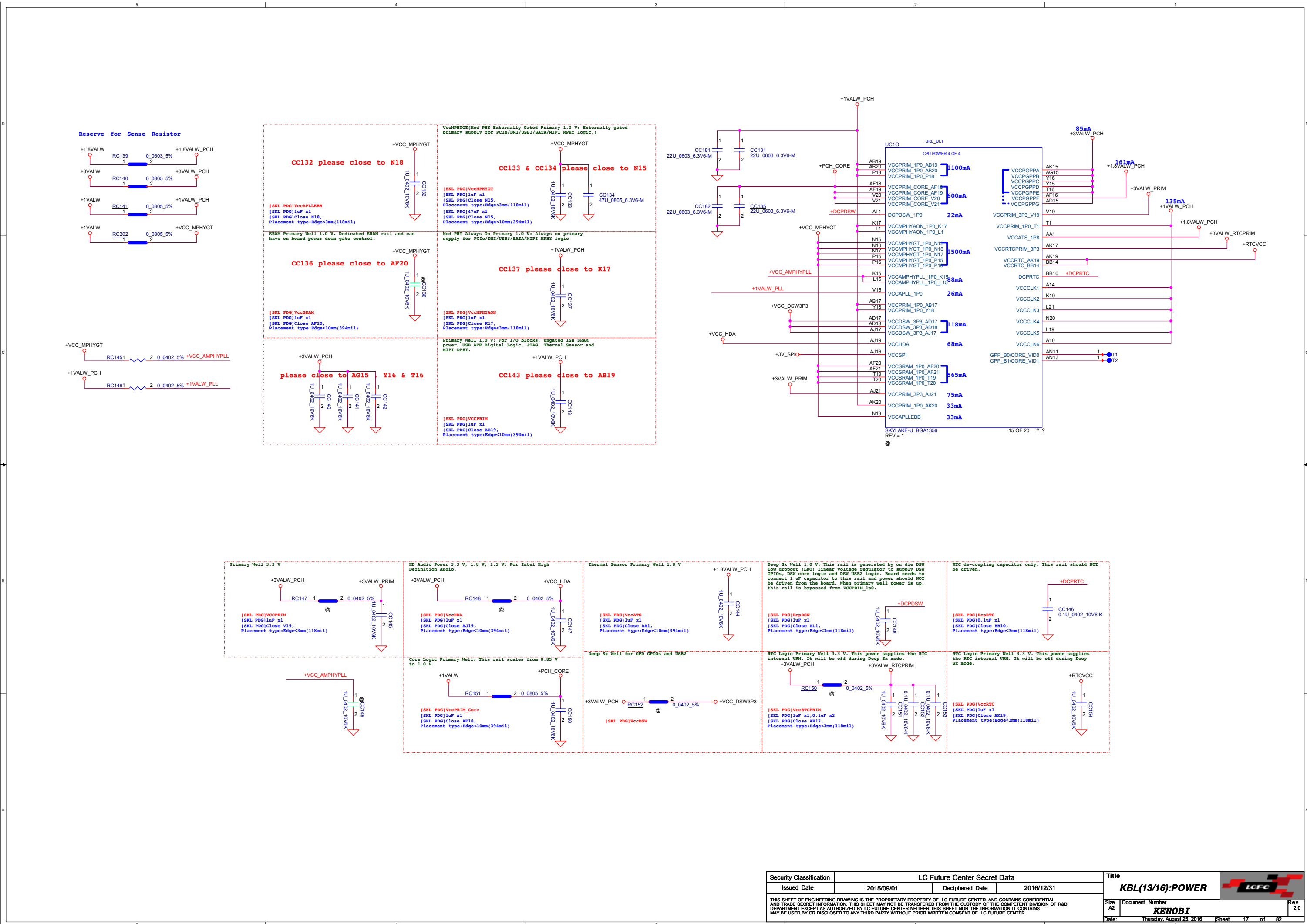


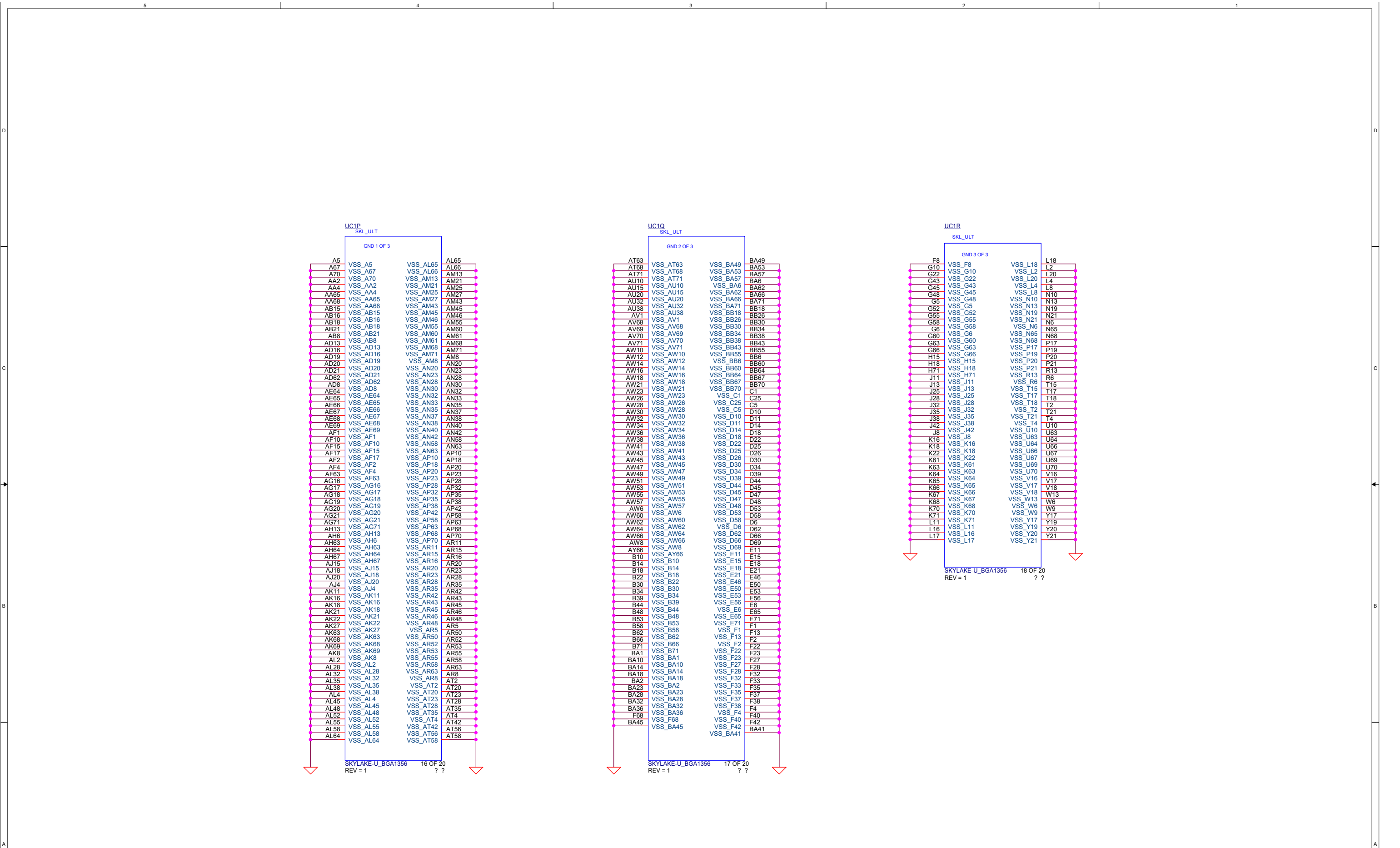


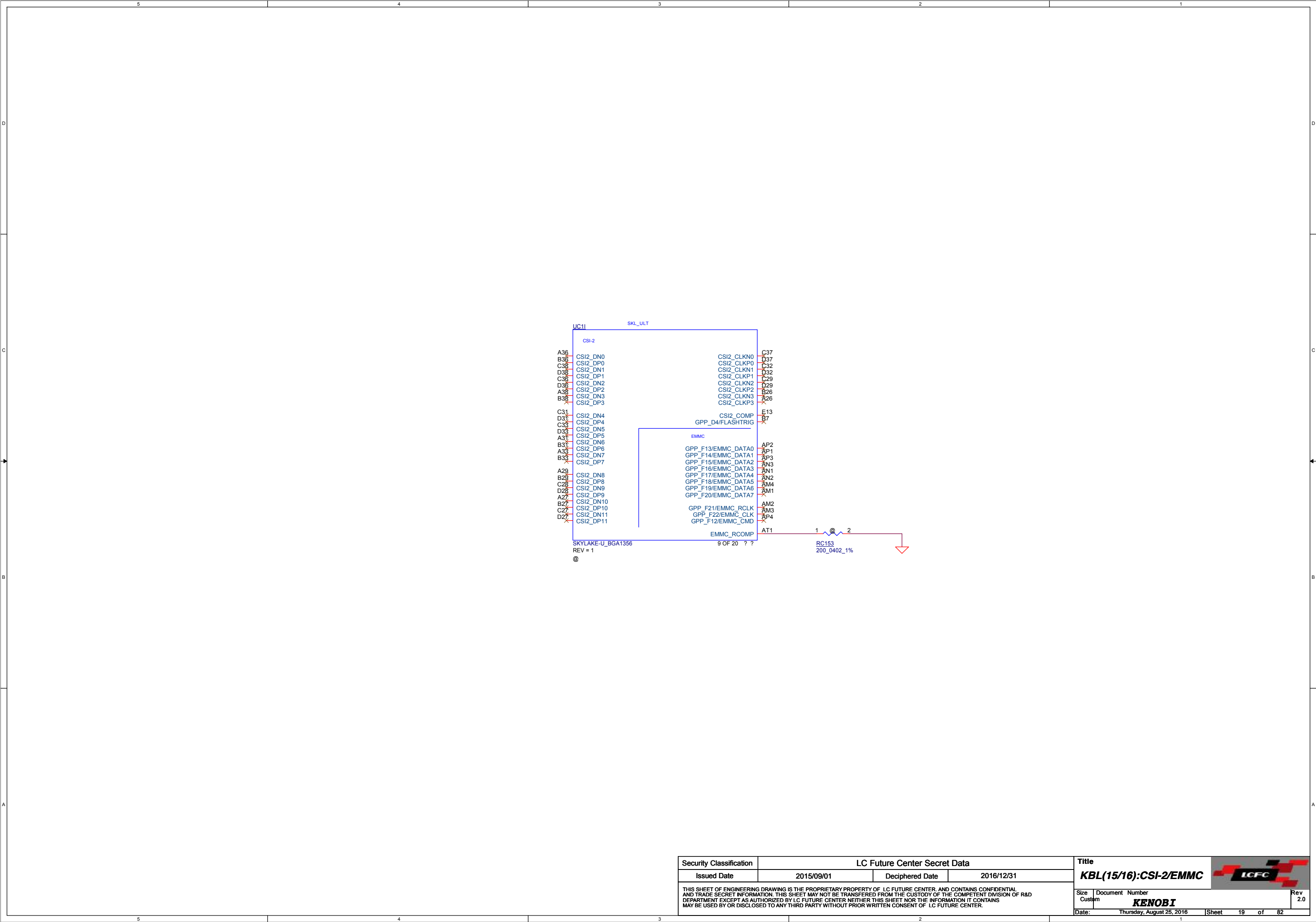


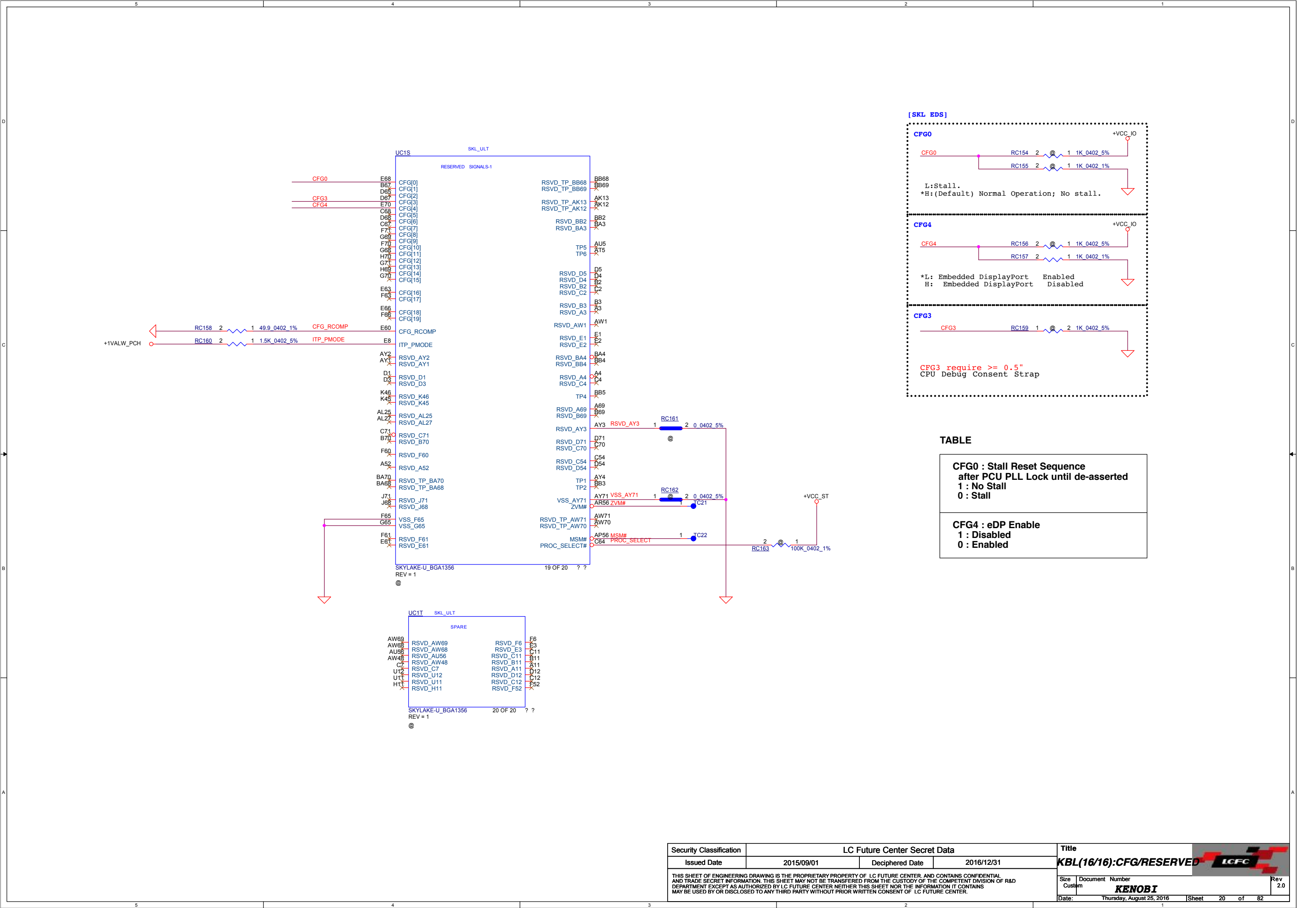
	USB Port Number
USB_OC0#	Reserve
USB_OC1#	Port2
USB_OC2#	Port3
USB_OC3#	Port4

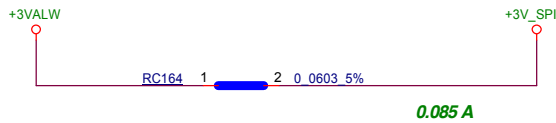




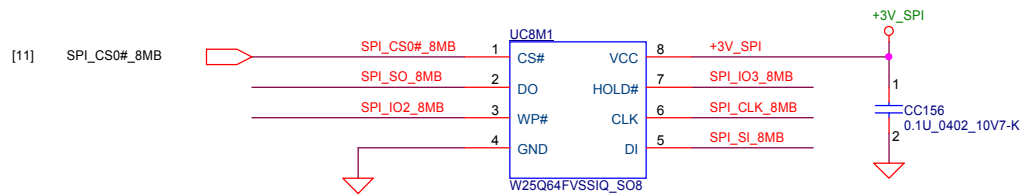




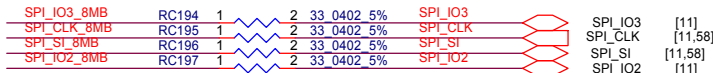




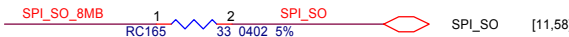
4MB(32Mb) Reserve



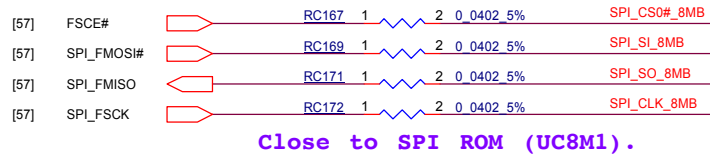
Place RC194,195,196,197 close together



Near SPI ROM

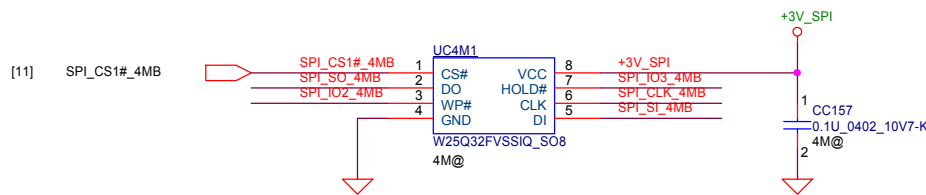


Mirror Code



8MB(64Mb)

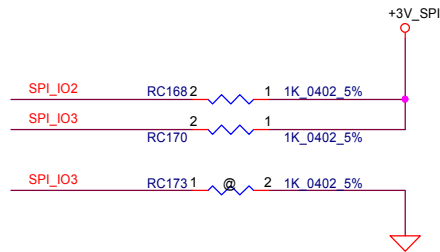
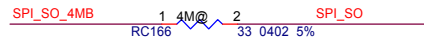
[94]SPI0_CS0# SPI FLASH
SPI0_CS1# SPI FLASH
SPI0_CS2# SPI TPM

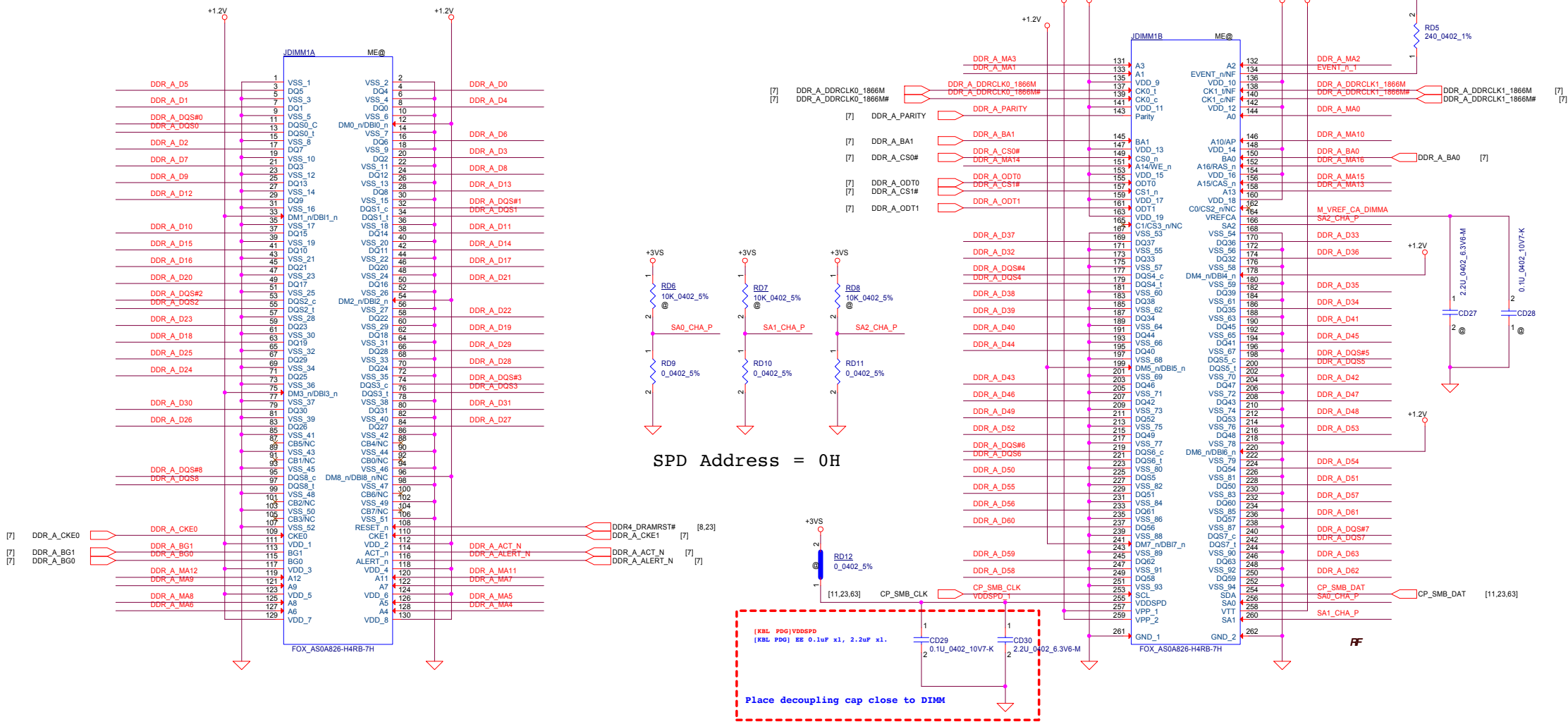
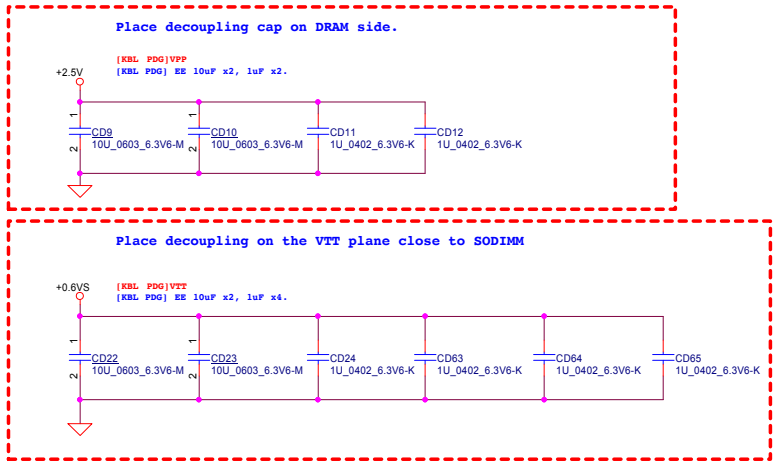
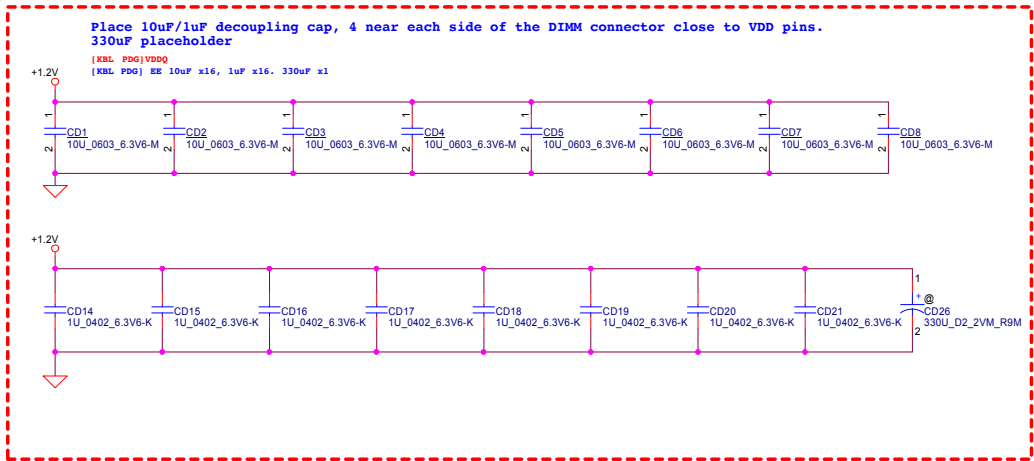


Place RC203,204,205,206 close together

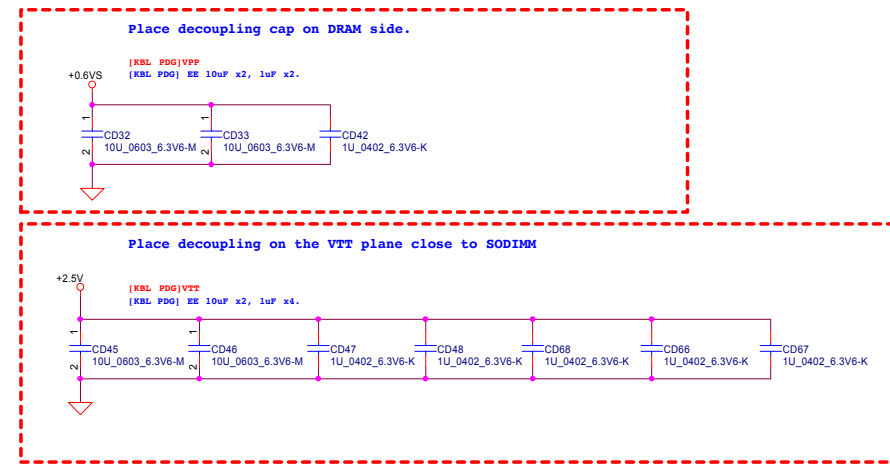



Near SPI ROM

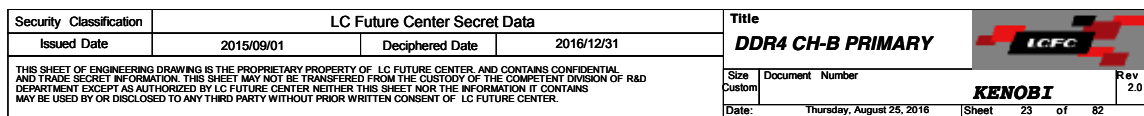




Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-R5	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors



	DDR_B_D[0..63]	[8]
	DDR_B_MA[0..16]	[8]
	DDR_B_DQS#[0..7]	[8]
	DDR_B_DQS[0..7]	[8]



Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_AON	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VS_AON	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_AON	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_AON	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VS_AON	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VS_AON				
STRAP3	+3VS_AON				
STRAP4	+3VS_AON				

X76

GPU	FB Memory (GDDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR	Samsung	K4W4G1646E-BC1A(E-Die)256MX16	PD 24.9K SD03424928T	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5TC4G63CFR-N0C(C-Die)256Mx16	PD 30.1K SD03430128T							
	Micron	MT41J256M16LY-091G:N	PD 20K SD02820028T							

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Issued Date		2015/10/5	Deciphered Date	2016/12/31	VGA NOTE
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Size B	Document Number			Rev 2.0	
Date:		Thursday, August 25, 2016		Sheet 24 of 82	

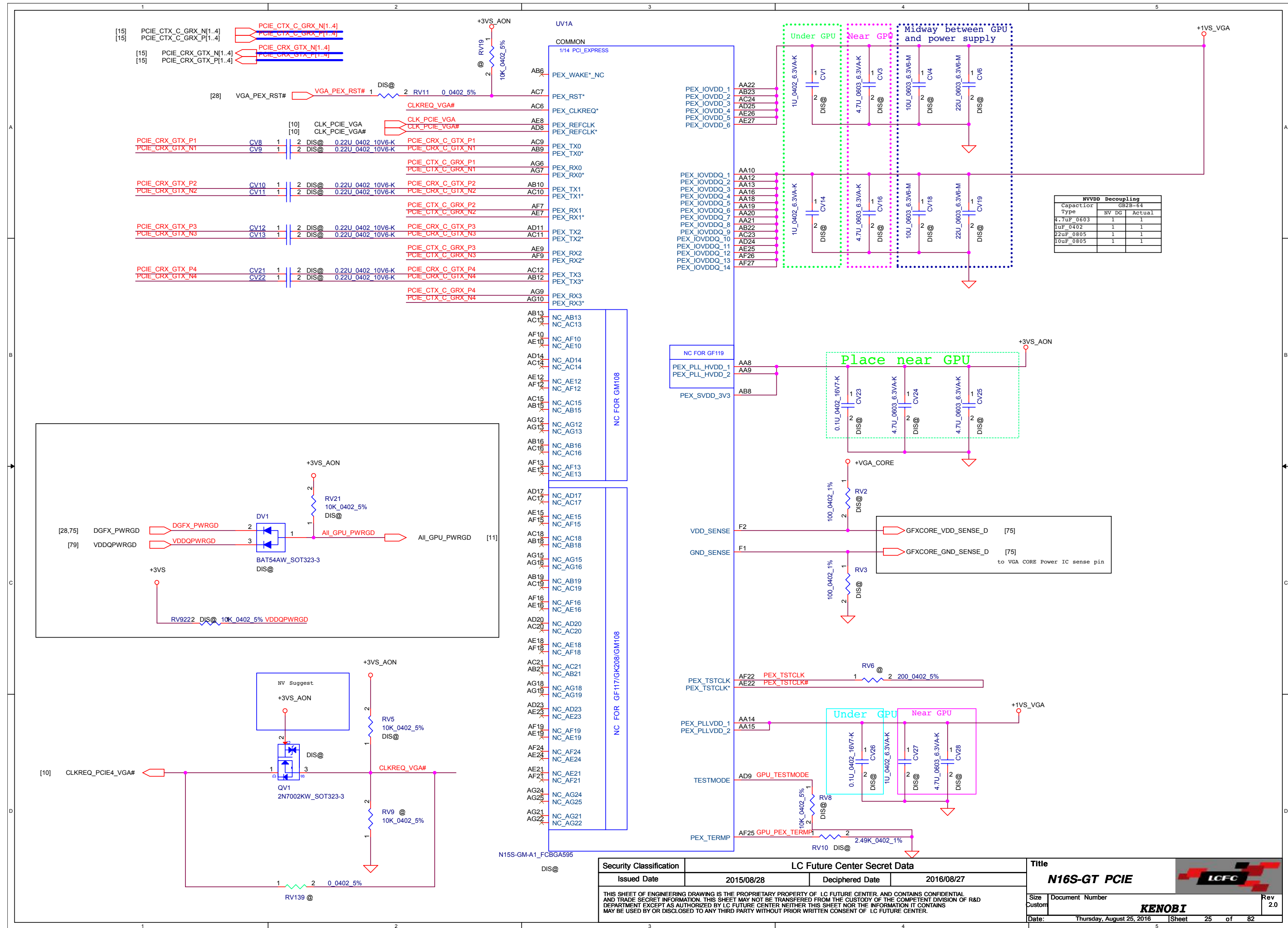
5

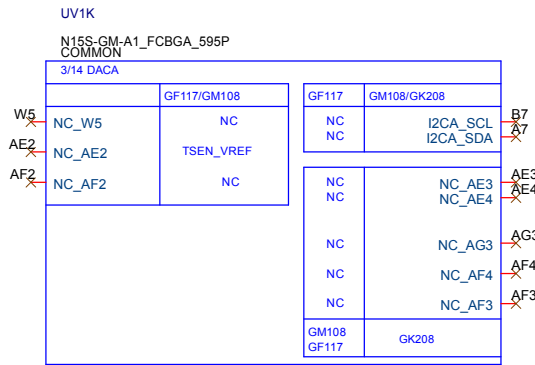
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3

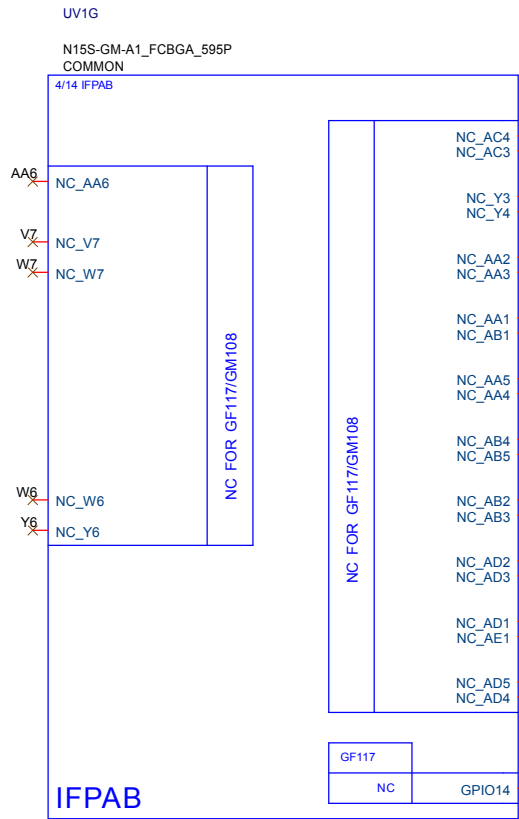
2

1

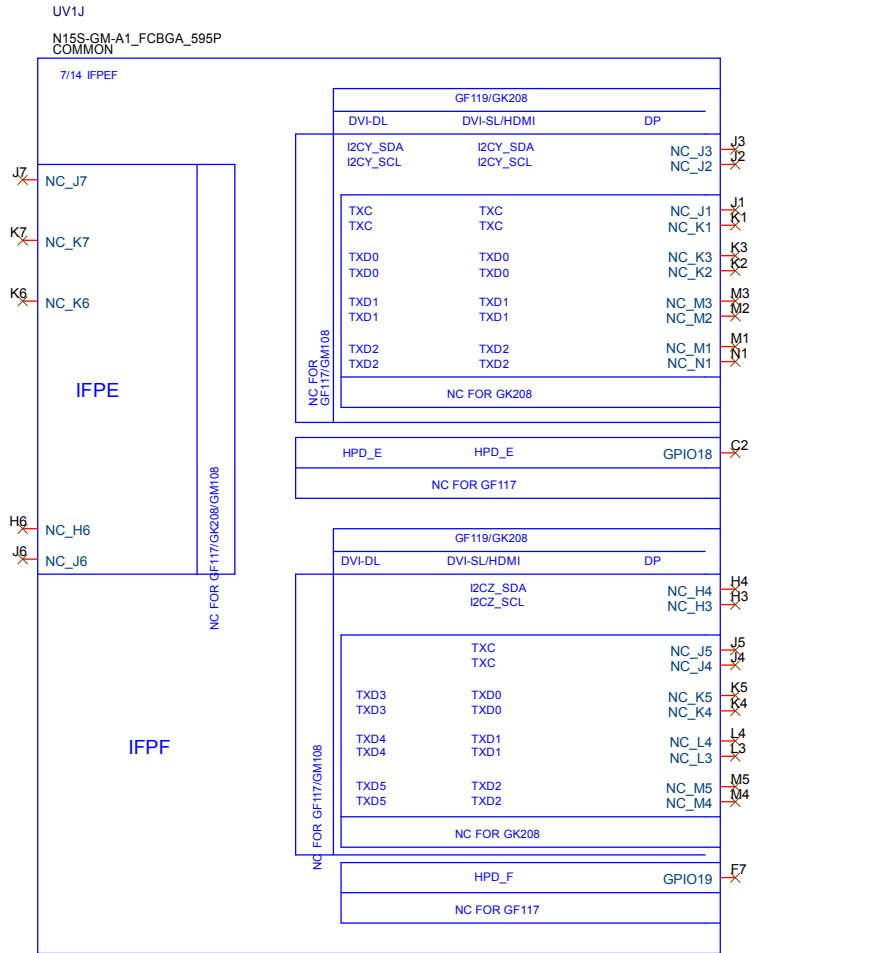




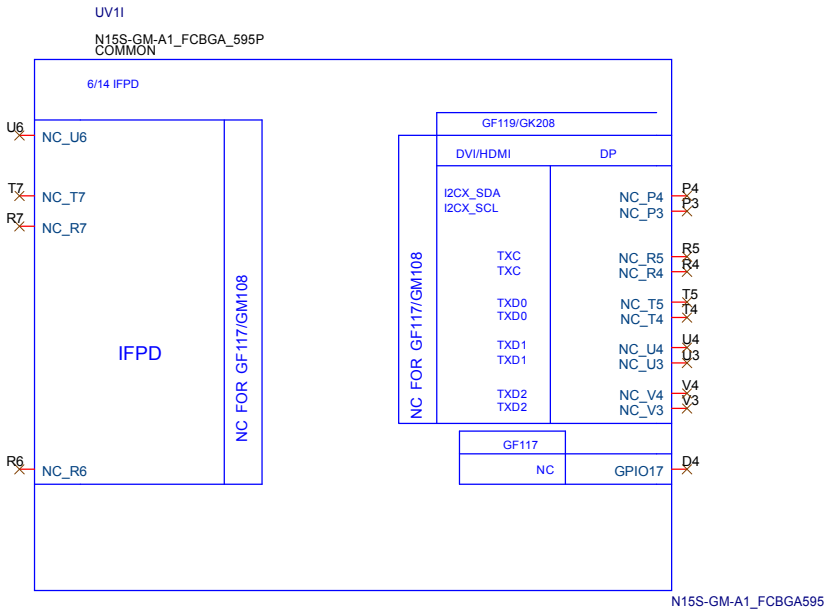
N15S-GM-A1_FCBGA595



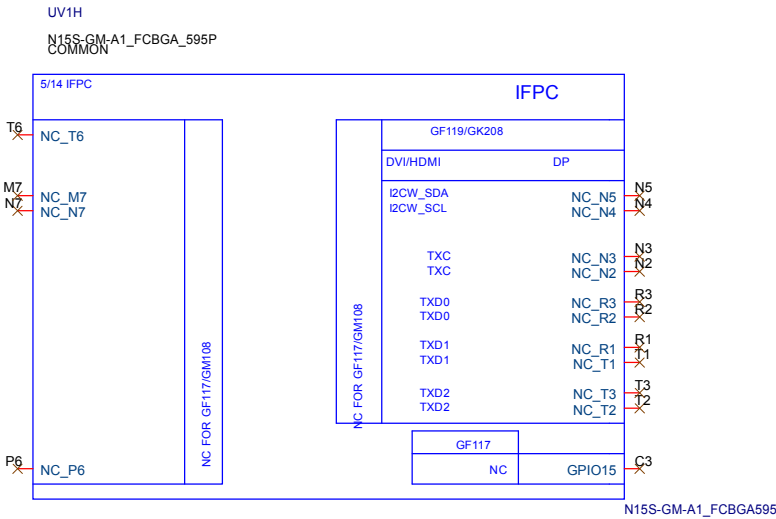
N15S-GM-A1_FCBGA595



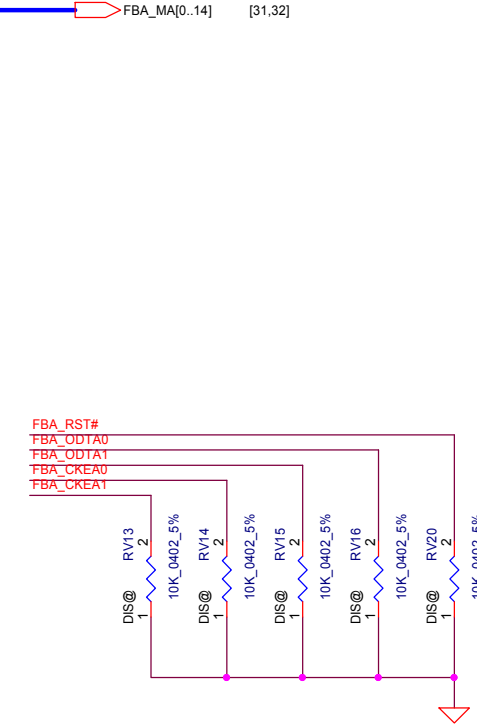
N15S-GM-A1_FCBGA595

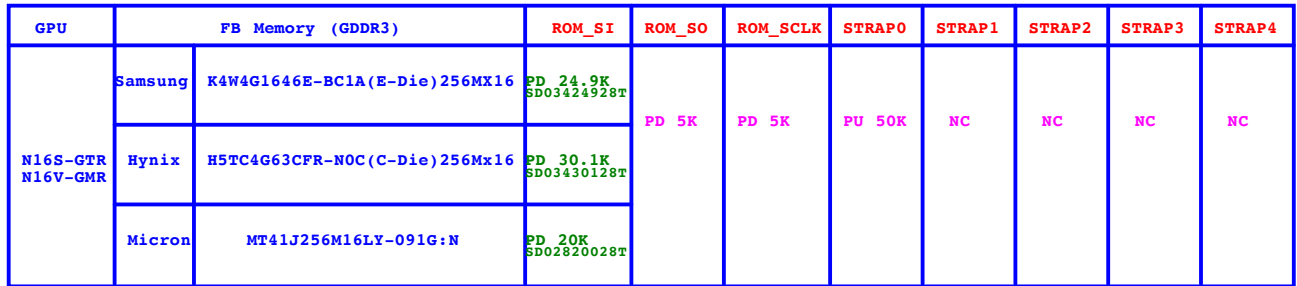




N15S-GM-A1_FCBGA595

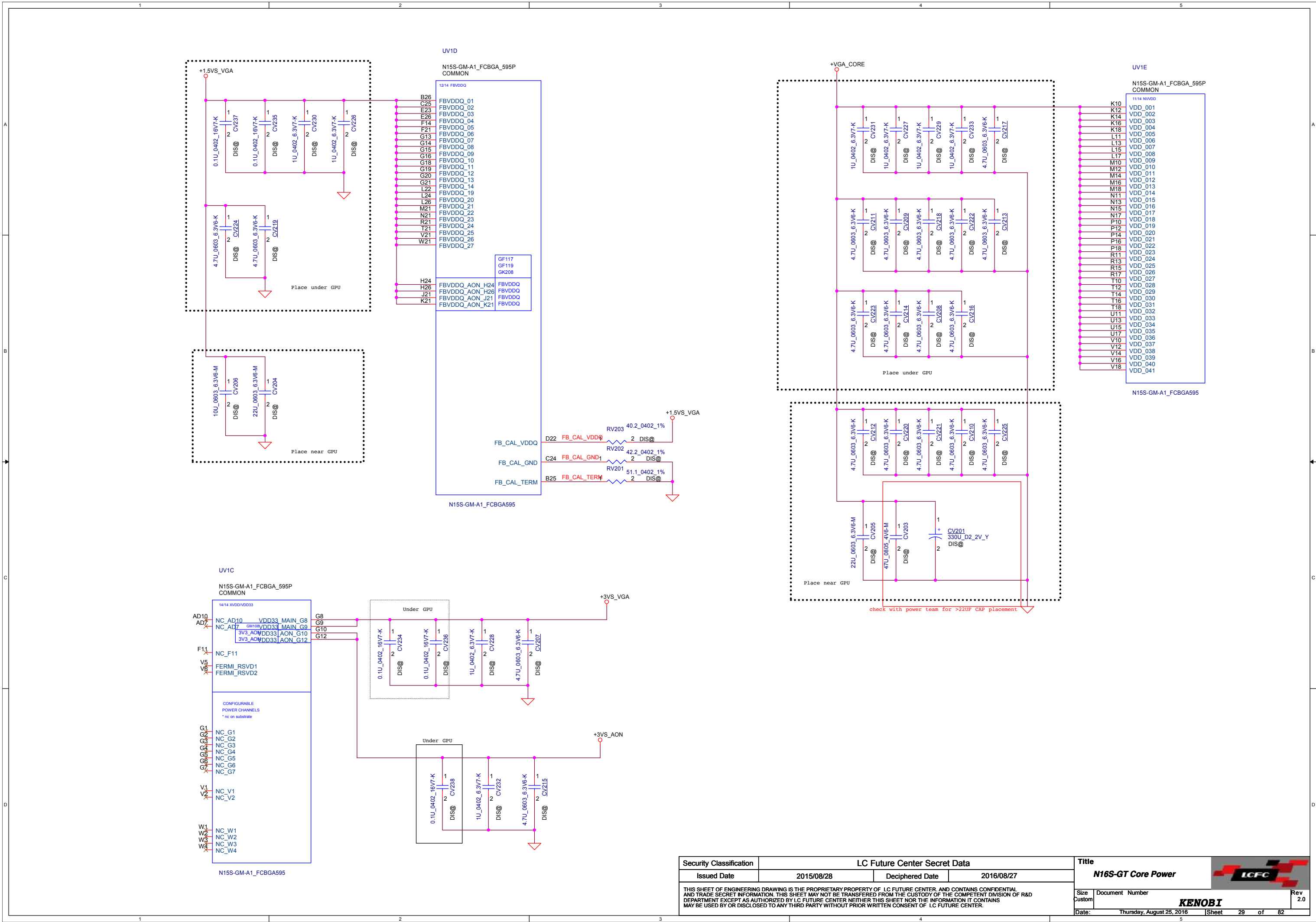


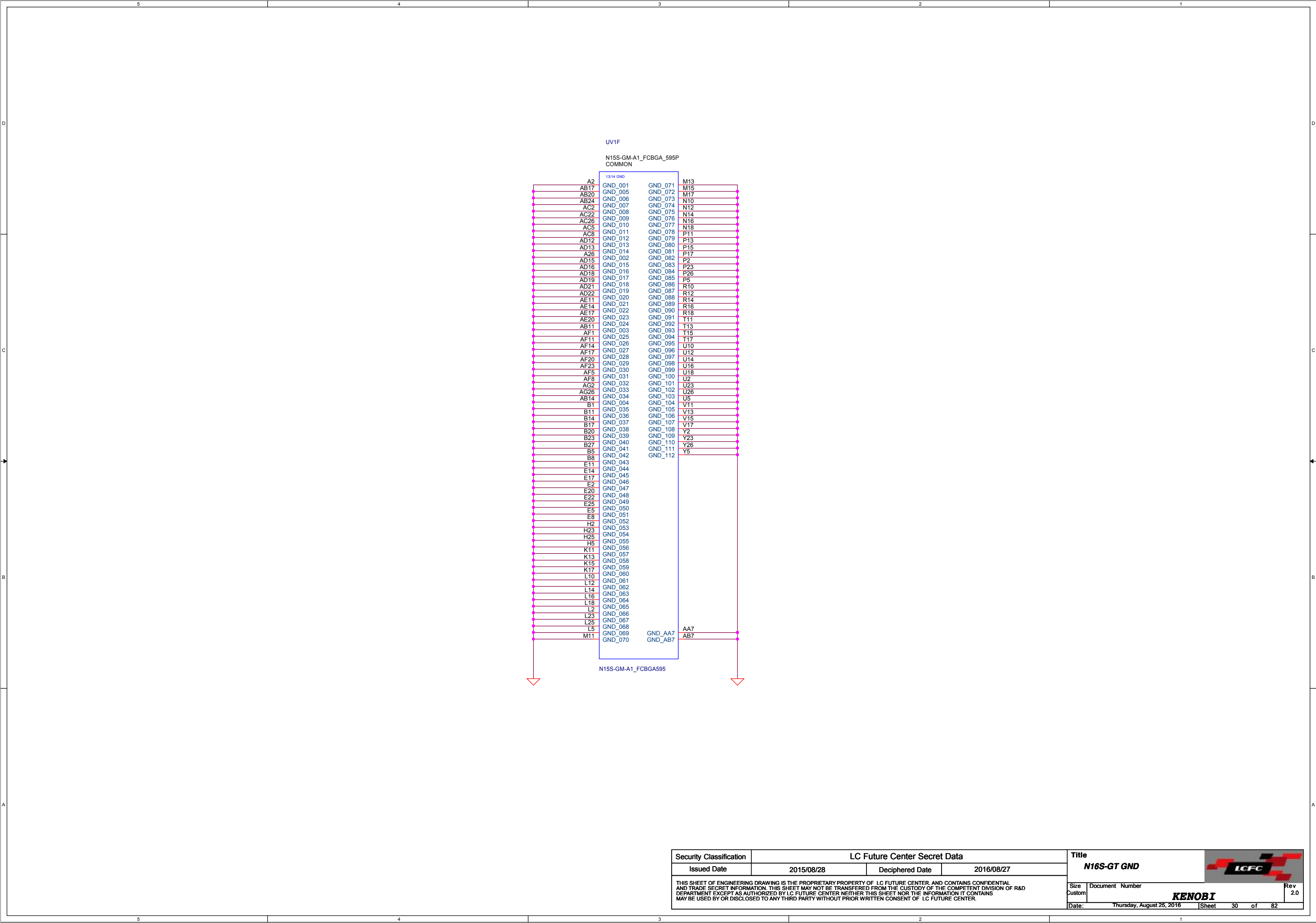
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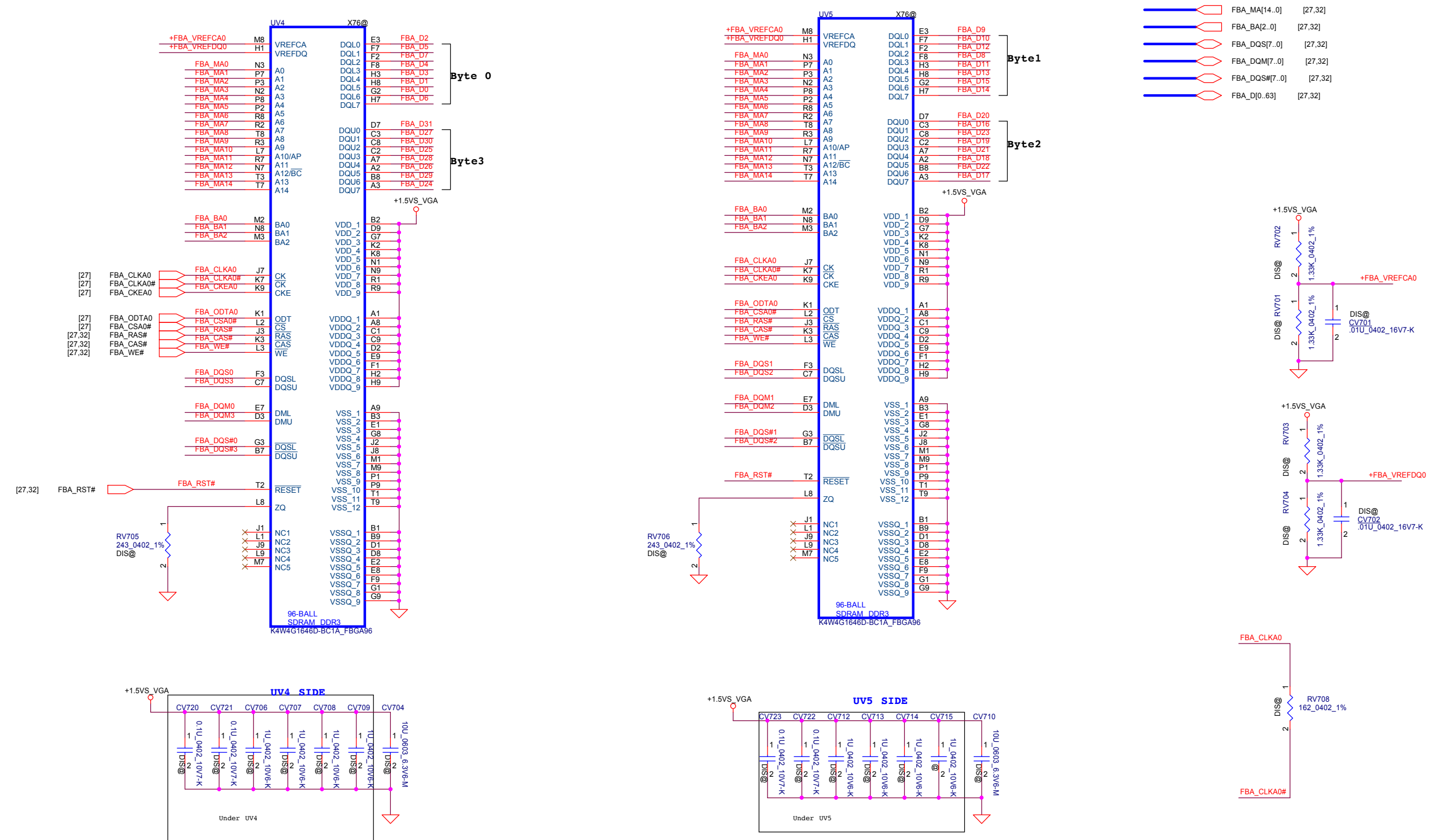



Security Classification		LC Future Center Secret Data		Title			
Issued Date	2015/08/28	Deciphered Date	2016/08/27	N16S-GT GPIO			
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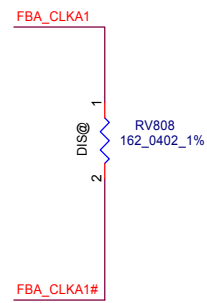
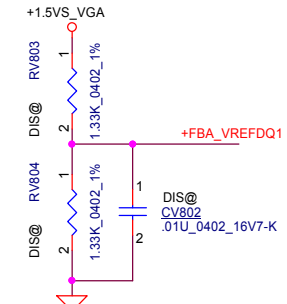
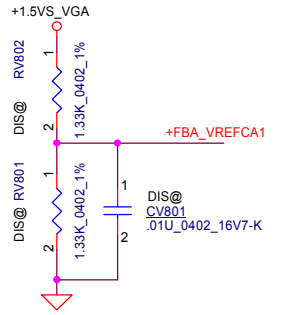
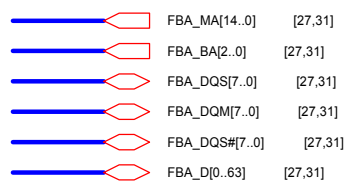
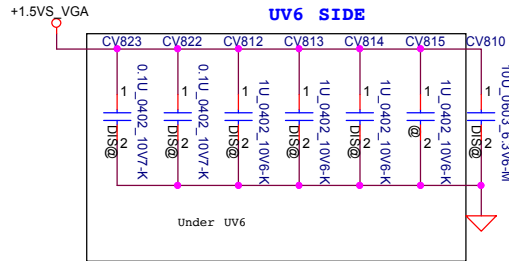
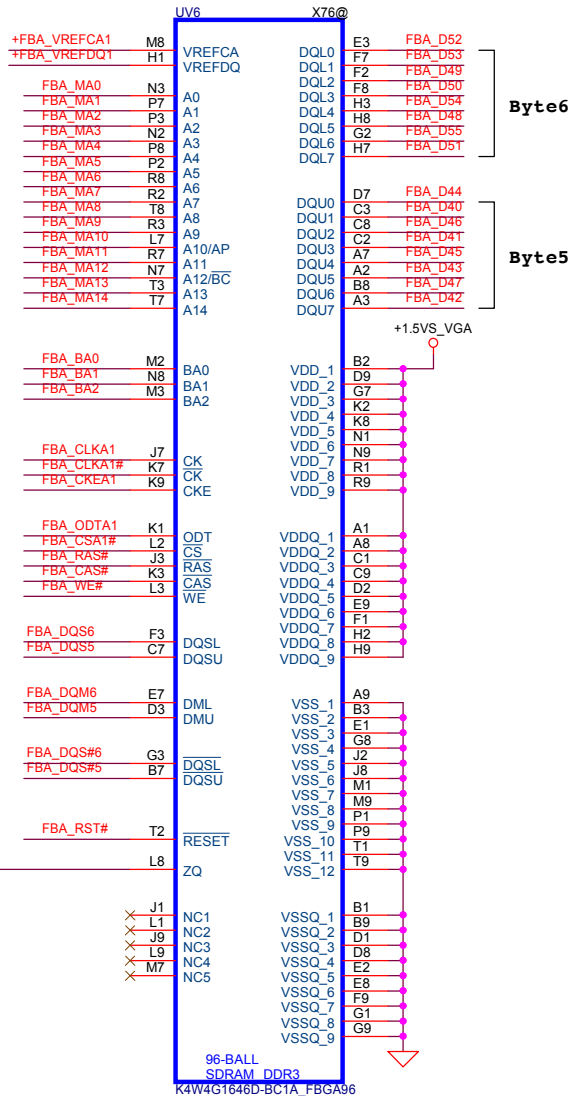
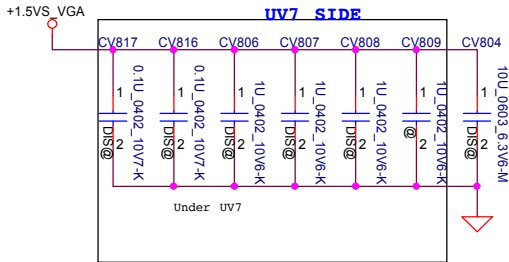
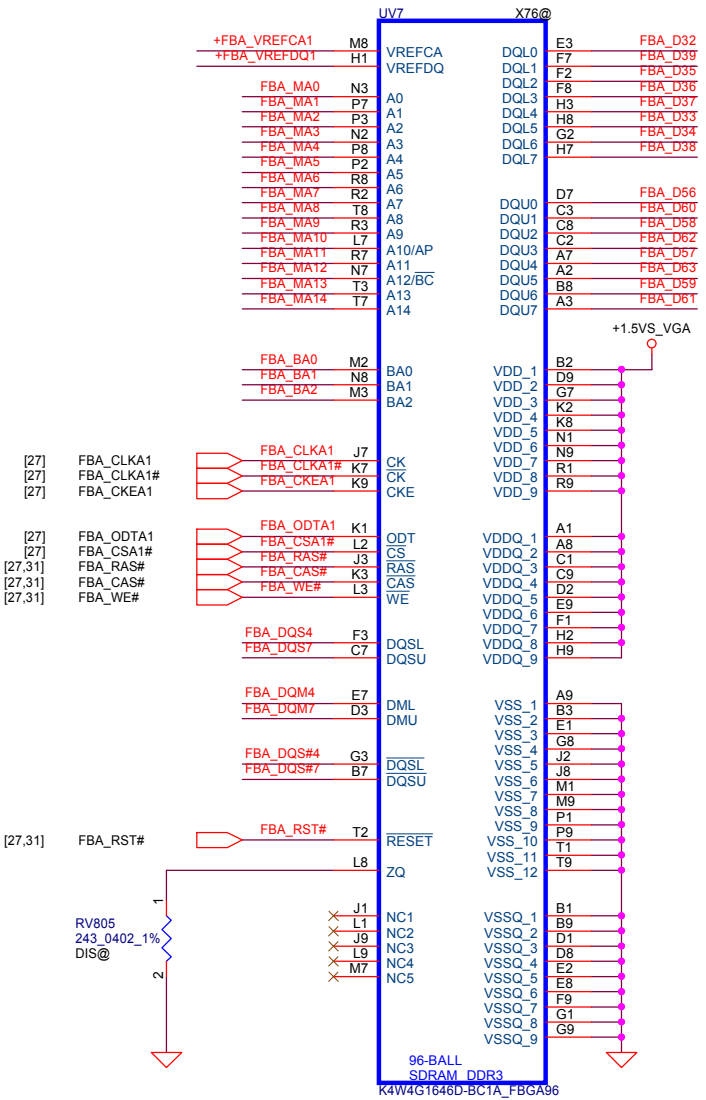


Memory Partition A - Lower 32 bits

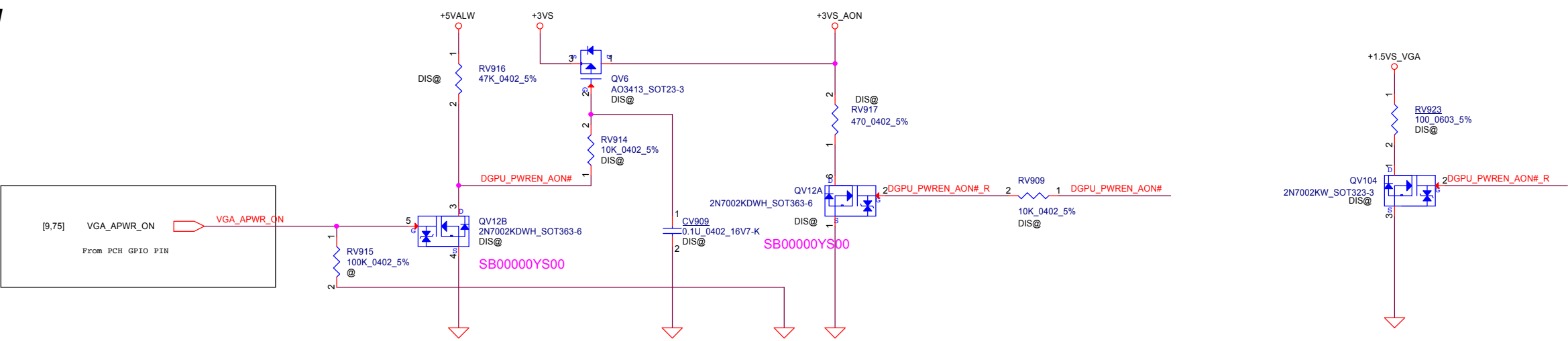


Security Classification		LC Future Center Secret Data		Title			
Issued Date	2015/08/28	Deciphered Date	2016/08/27	N16S-GT DDR3L VRAM L			
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				Custom			2.0
				Date: Thursday, August 25, 2016		Sheet	31 of 82

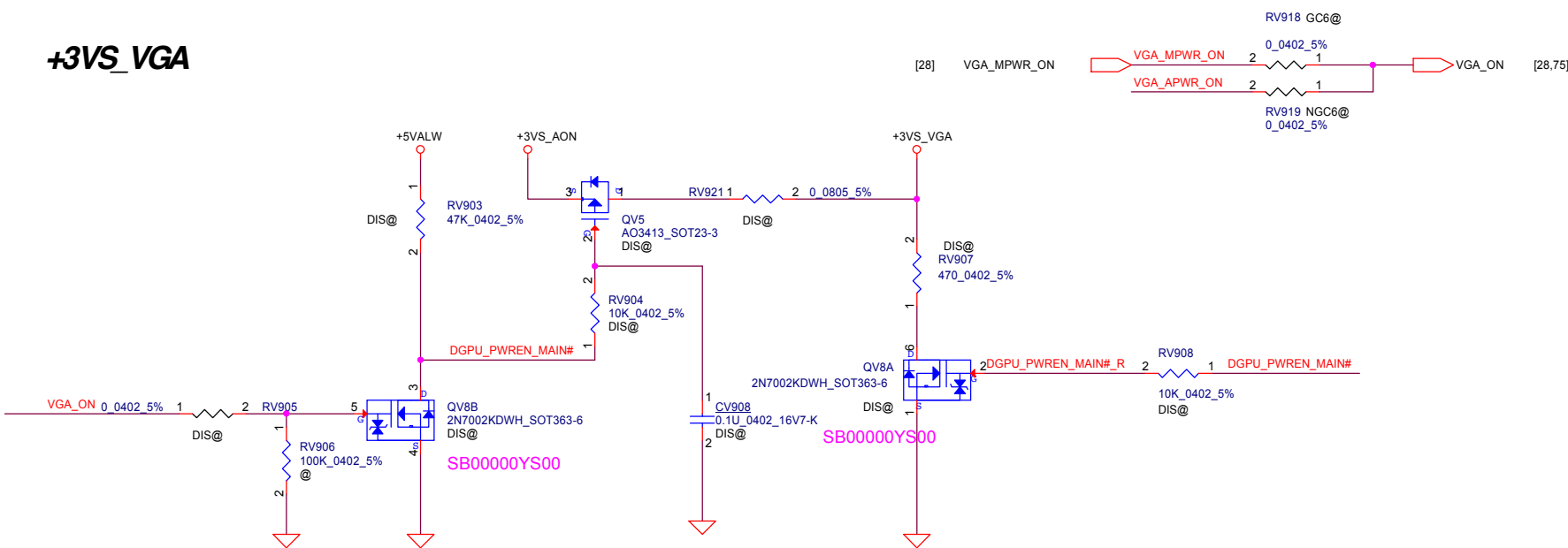
Memory Partition A - Upper 32 bits



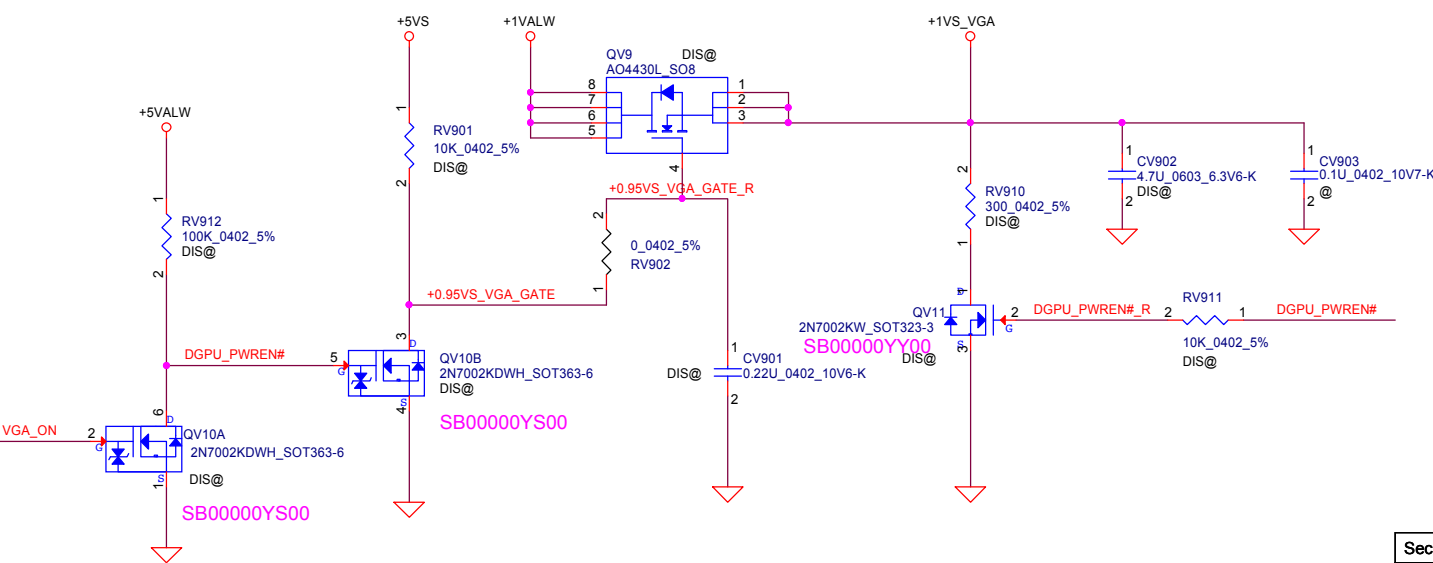
+3VSto +3VS_AON



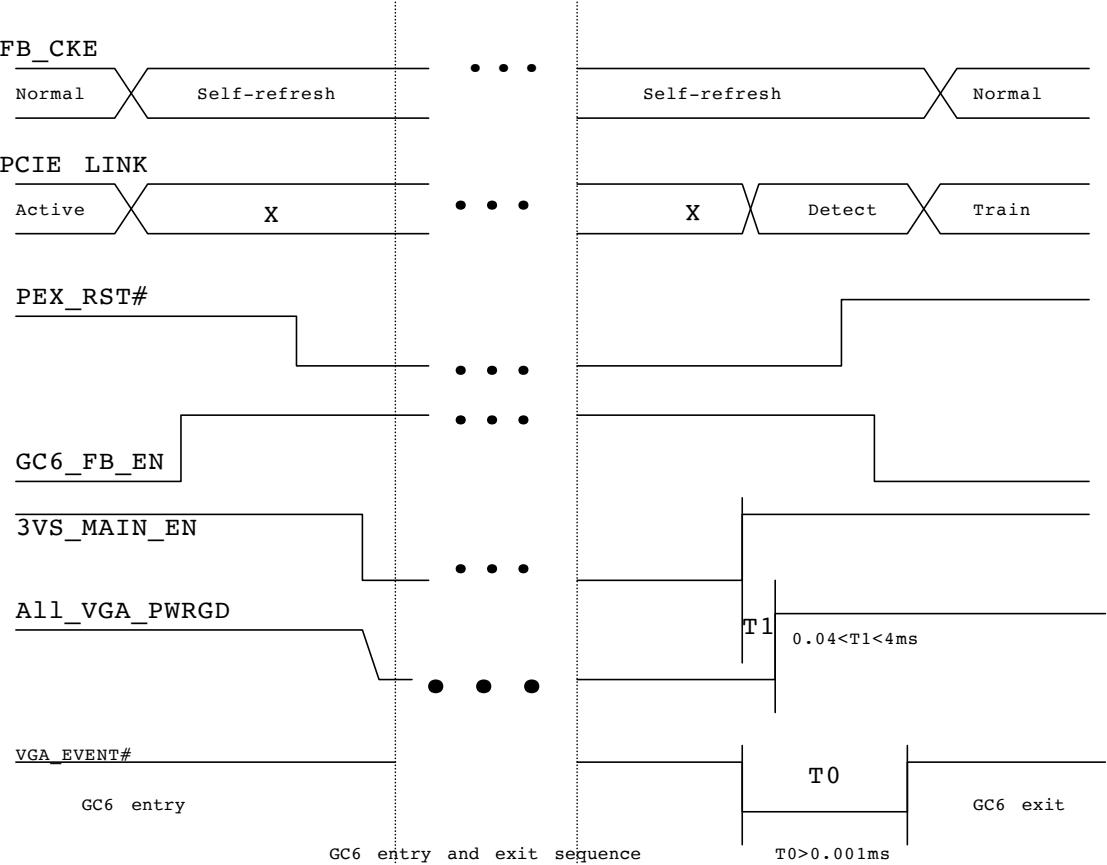
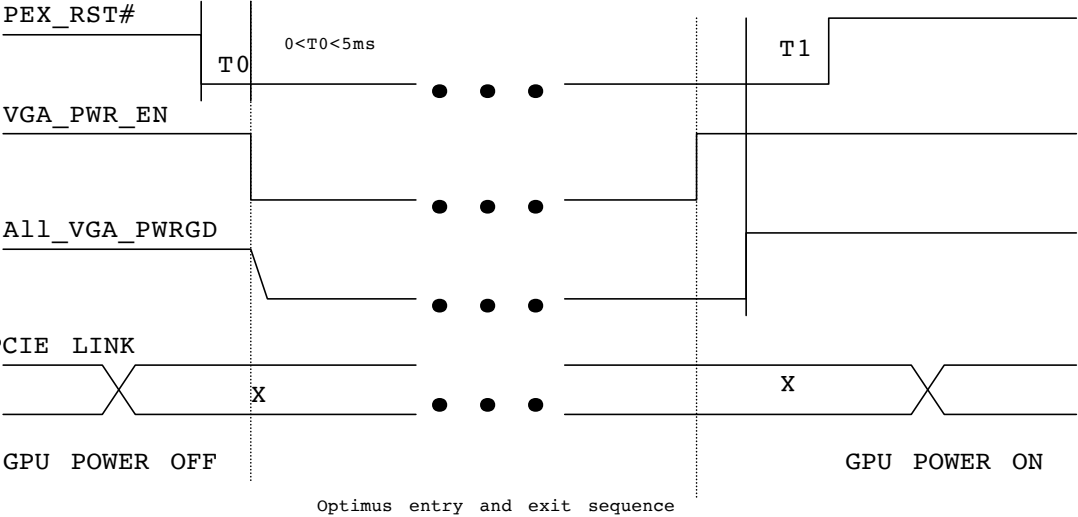
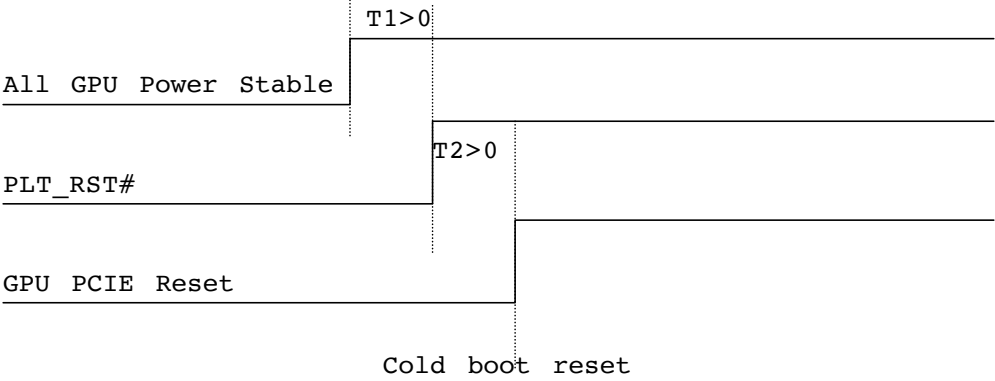
+3VS_VGA




+1VALW to +1VS_VGA

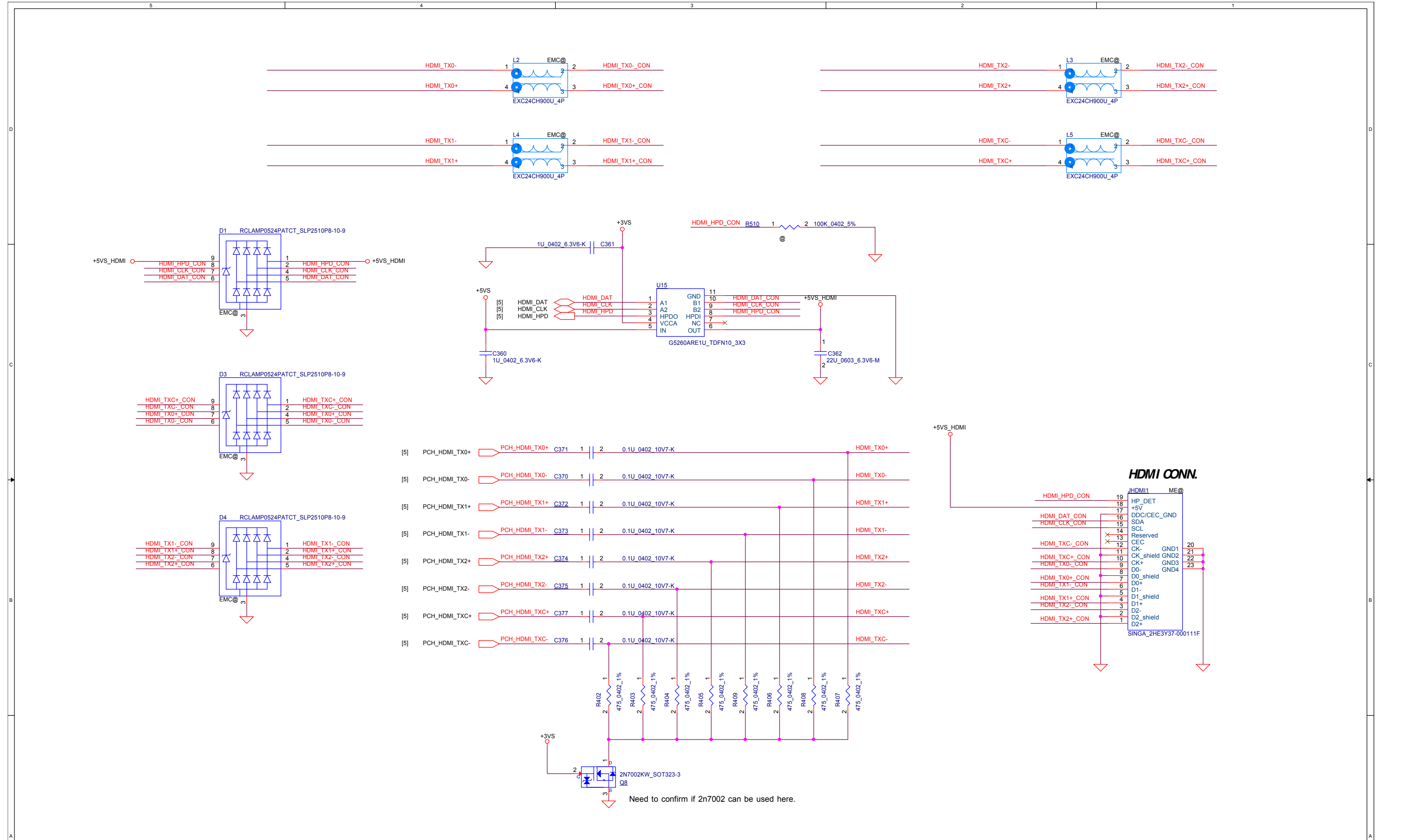


GPIO	I/O	Functional Description	I/O Termination
GPI00	O	FB Enable for GC6 2.0, Open source	10K pull-down
GPI01	O	Memory voltage control	Pull-up/pull down to set the FBVDD/Q boot voltage
GPI02	O	Panel Backlight PWM Brightness Control	100K pull down
GPI03	O	Panel Power Enable	100K pull down
GPI04	O	Panel Backlight Enable	100K pull down
GPI05	O	GPU Power Sequence for GC6 2.0, Open Drain	10k pull-up to 3V3_AON
GPI06	I	GPU wake signal for GC6 2.0	10k pull-up to 3V3_AON
GPI07	O	3D Vision L/R signal	100K pull down
GPI08	O	System side PCIe rest monitor	10k pull-up to 3V3_AON
GPI09	I/O	Active low thermal alert, open drain	10k pull-up to 3V3_AON
GPI010	O	Memory VREF Control	100K pull down
GPI011	O	GPU Core VDD PWM control signal	
GPI012	I	AC power detect or power supply overdraw input	100k pull-up to 3V3_AON
GPI013	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase
GPI014	I	Hot Plug Detect for IFPA used as DisplayPort for IFPAB when used as Dual Link DVI	
GPI015	I	Hot Plug Detect for IFPC	
GPI016	I	Active Low Frame Lock, Open Drain	10k pull-up to 3V3_AON
GPI017	I	Hot Plug Detect for IPFD	
GPI018	I	Hot Plug Detect for IPFE	
GPI019	I	Hot Plug Detect for IPFF or for IPFB when used as DisplayPort	
GPI020	O	Reserved	
GPI021	O	GPU PCIe self-reset control, Open Drain	10k pull-up to 3V3_AON
OVERT	I/O	Catastrophic Over Temperature	100k pull-up to 3V3_AON



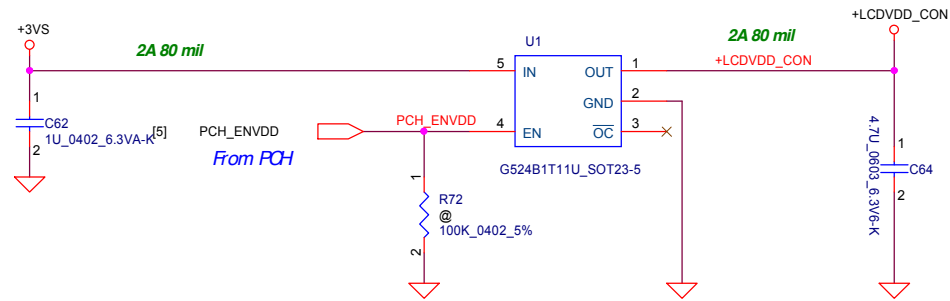
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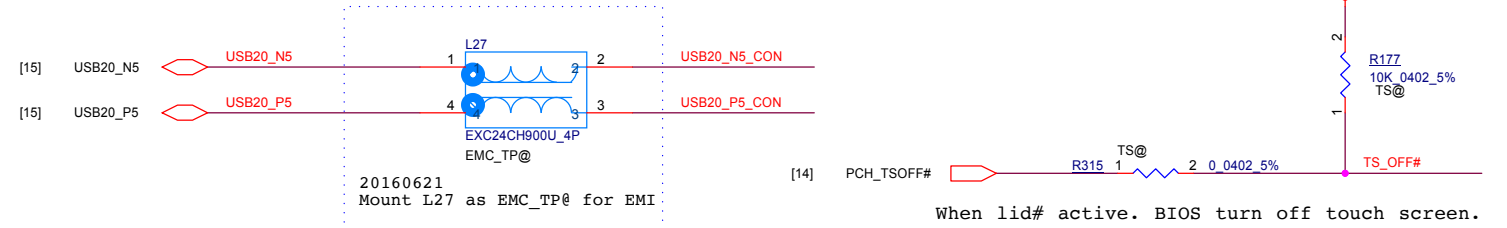


Need to confirm if 2n7002 can be used here.

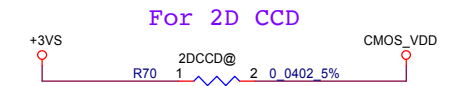
LCDVDD Circuit



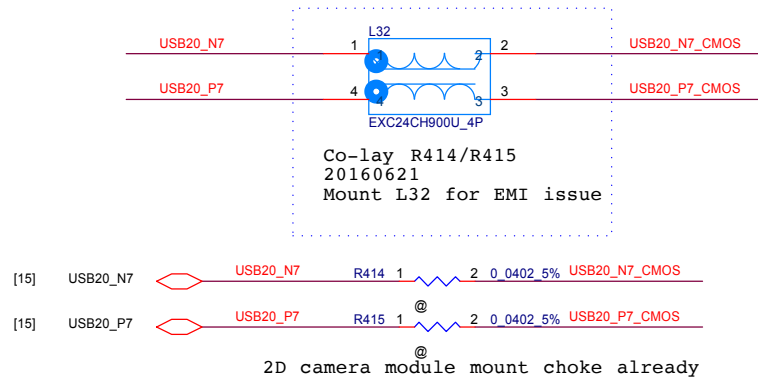
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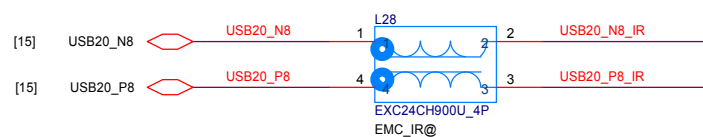
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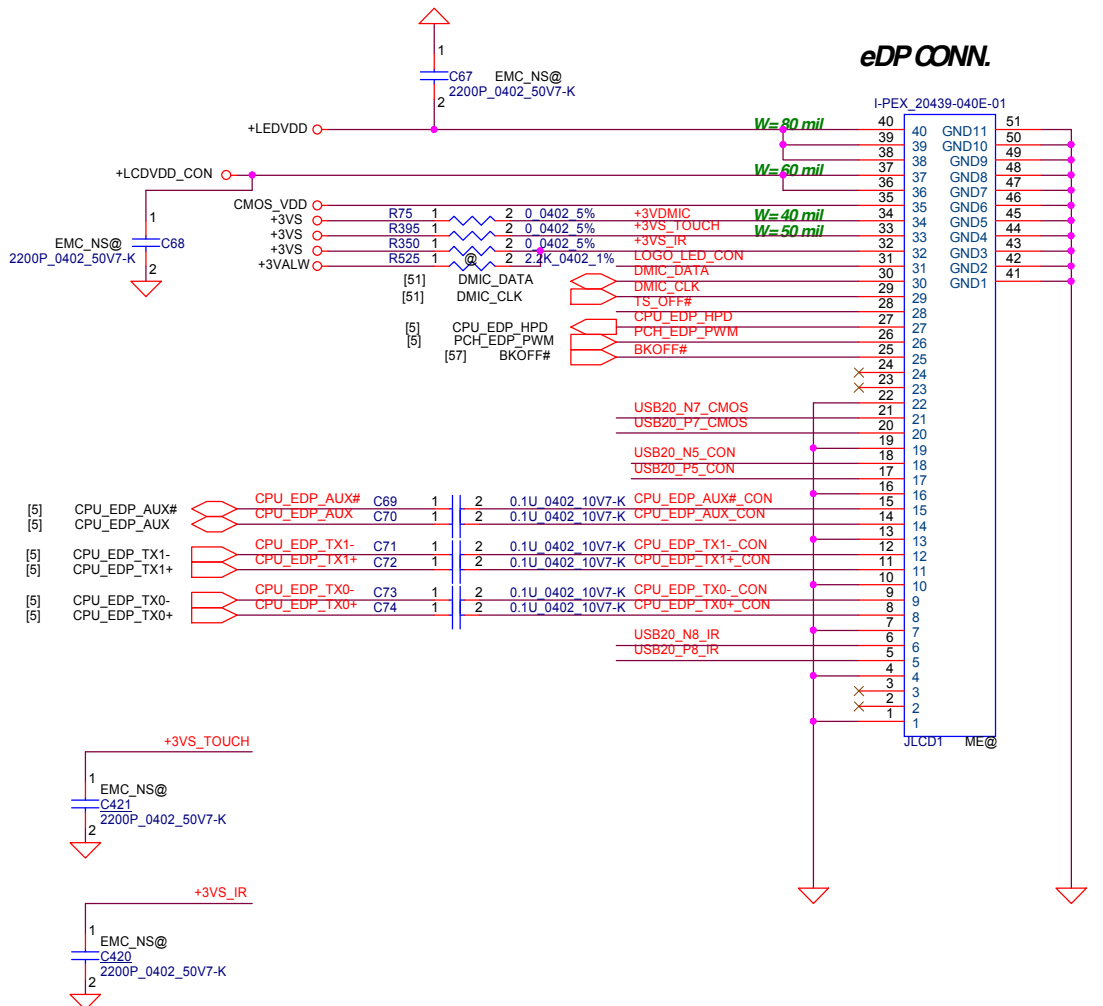
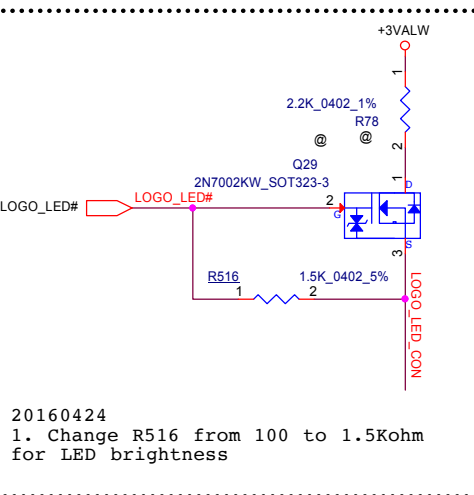
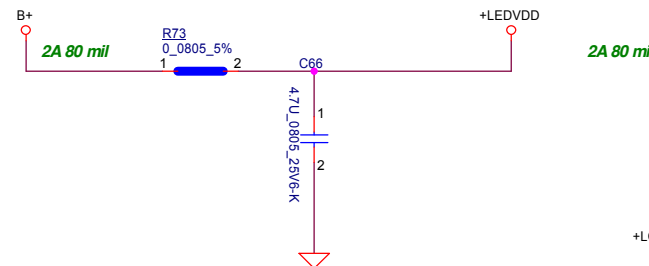
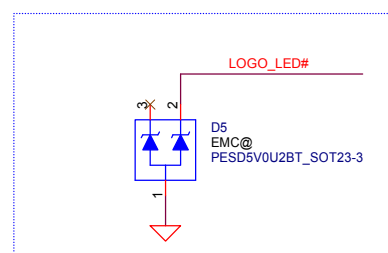
CMOS USB Port



IR camera USB Port



ESD request



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LC Future Center Secret Data				eDP CONN	
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				Date:	Thursday, August 25, 2016
				Sheet	37 of 82
				Rev	2.0

The image shows a large, mostly blank sheet of paper, likely a technical drawing or engineering blueprint. At the top, there is a horizontal grid header with labels 5, 4, 3, 2, and 1 from left to right. On the left side, there is a vertical grid header with labels D, C, B, and A from top to bottom. In the center of the page, the word "BLANK" is written in large, bold, black capital letters.

In the bottom right corner, there is a technical drawing title block. It contains the following information:

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Issued Date	2015/10/5	Deciphered Date	2014/09/07	HDMI RP	
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				Date: Thursday, August 25, 2016	Rev 2.0

Below the title block, there is a footer row with the text: "Sheet 38 of 82".

A

B

C

D

5


4

3

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1

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Issued Date	2015/10/5	Deciphered Date	2016/12/31	CRT CONN			
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Date:	Thursday, August 25, 2016			Sheet	39	of	82

5


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Issued Date		2015/10/5	Deciphered Date	2016/12/31			DP to VGA	
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						KENOBI		
Date:						Thursday, August 25, 2016	Sheet 40	of 82

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Issued Date	2015/10/5	Deciphered Date	2016/12/31	Mux IC		
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A

B

C

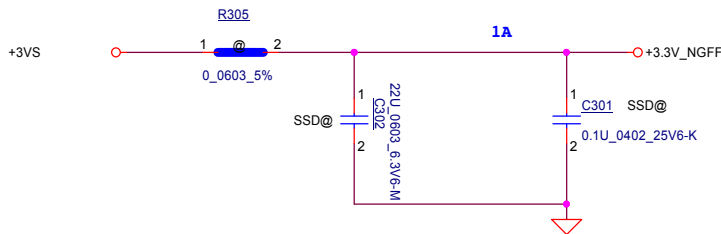
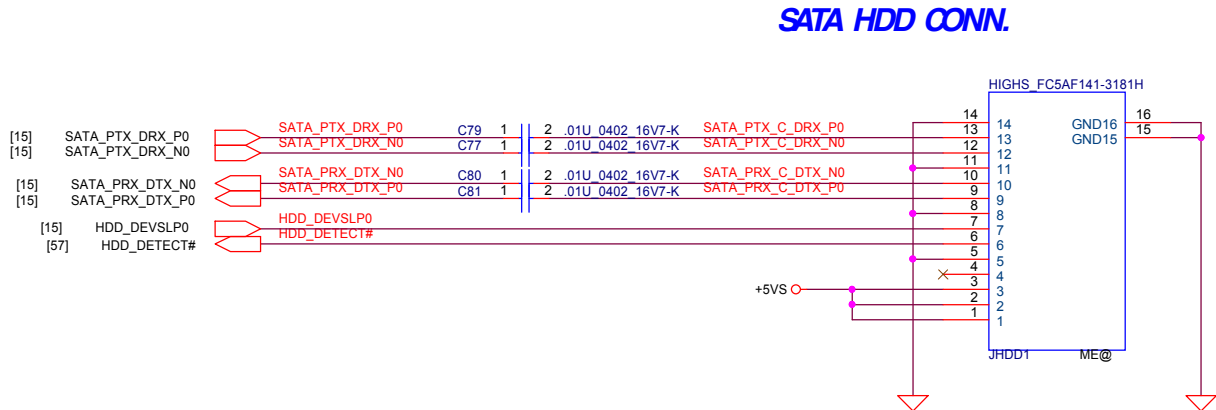
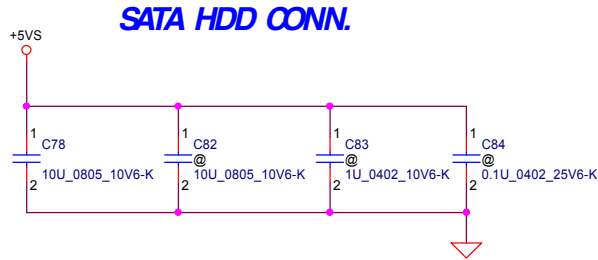
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E

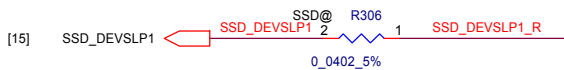
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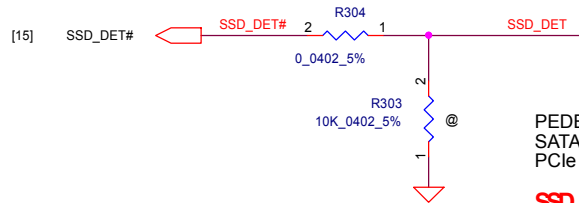
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M.2 SSD(SATA/PCIE)

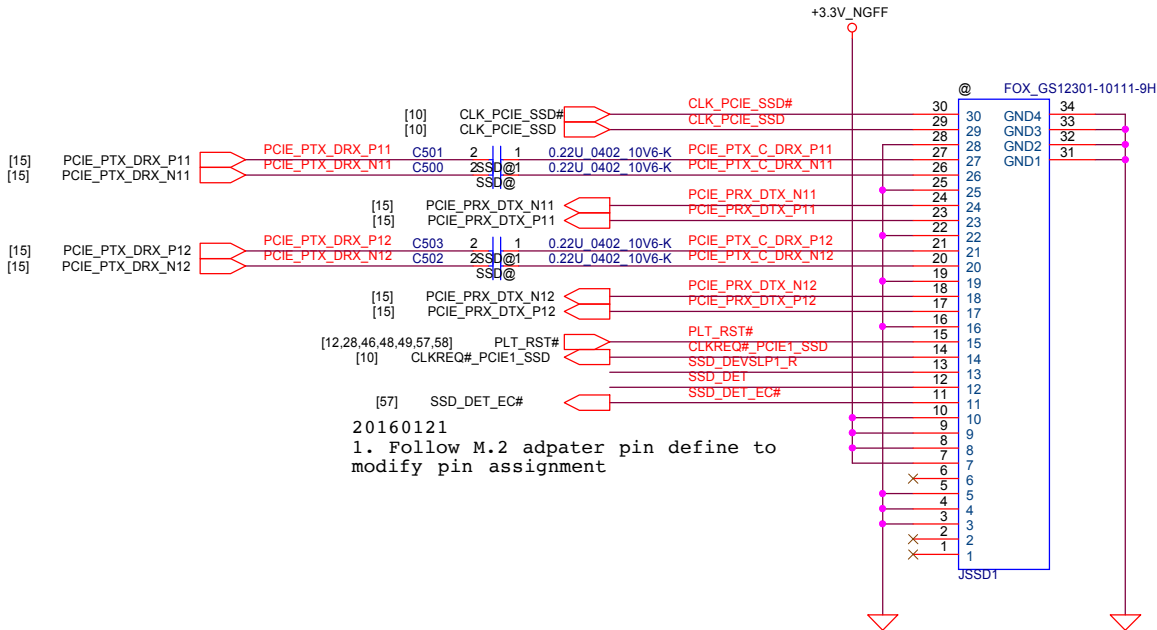


20160308
1. Remove R300,R301,R302 and put it to CPU side







PEDET (PE_DTCT)
SATA Device GND
PCIe Device Open

SSD_DET#
0 - SATA
1 - PCIE



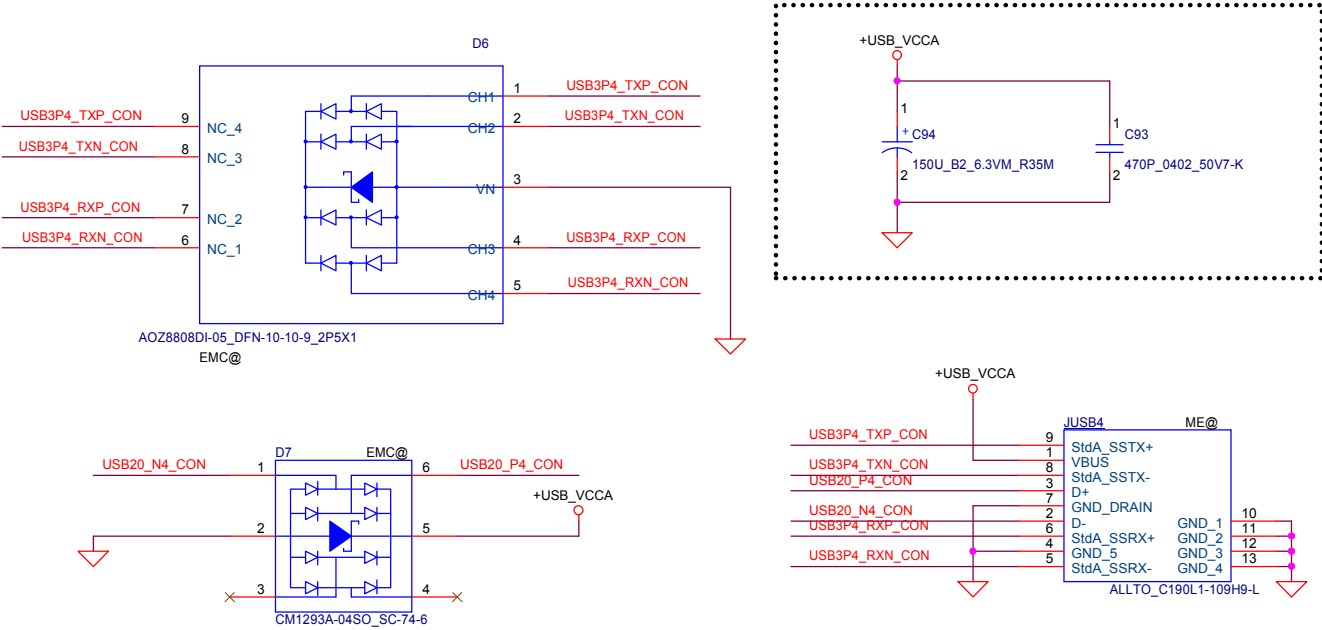
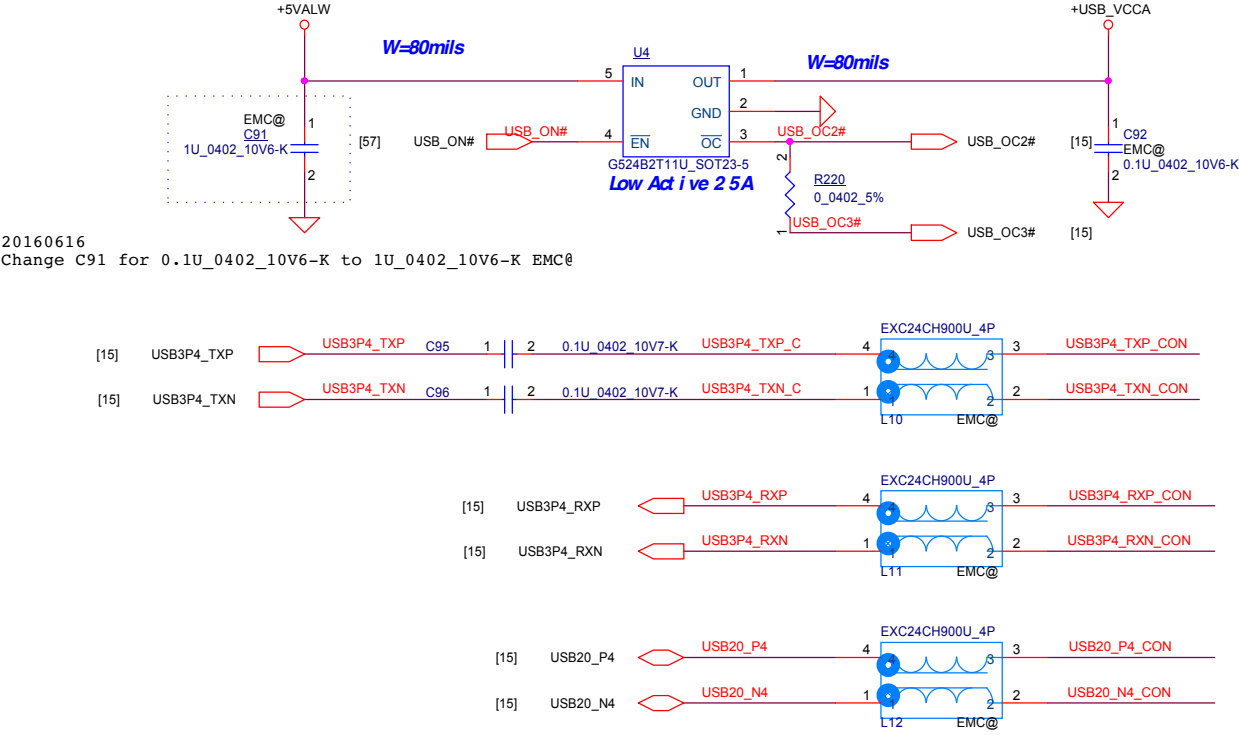
20160121
1. Follow M.2 adapter pin define to modify pin assignment

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						Date:	Thursday, August 25, 2016	Sheet 42 of 82

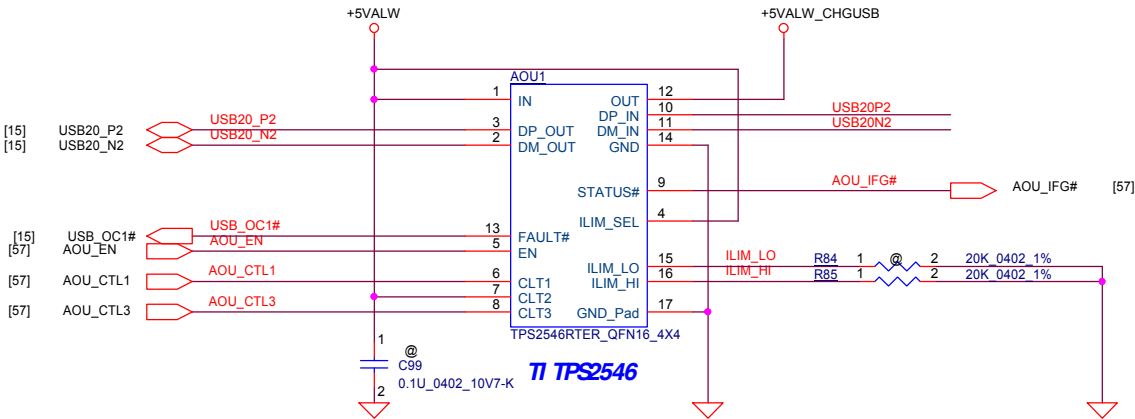
5	4	3	2	1																									
D				D																									
C				C																									
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Issued Date	2015/10/5	Deciphered Date	2016/12/31	ODD																									
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Date: Thursday, August 25, 2016					Sheet 43 of 82																								
5	4	3	2	1																									

USB3 PORT4

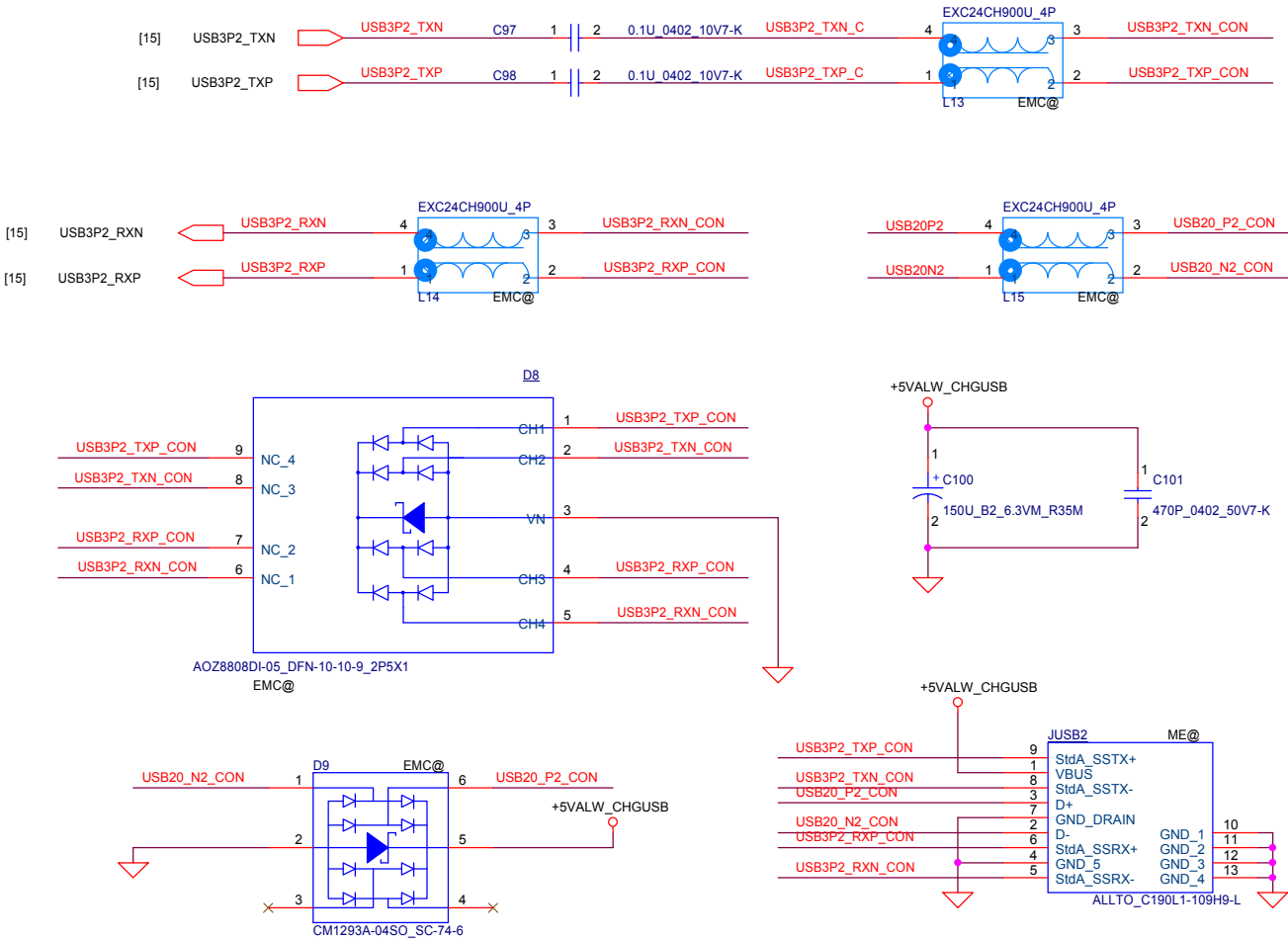
POWER SWITCH



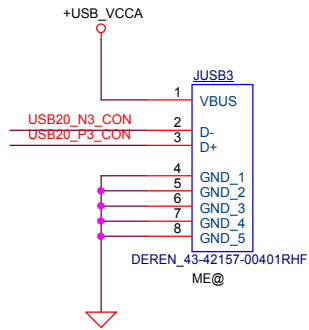
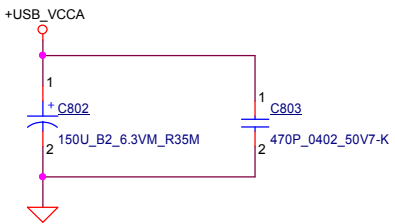
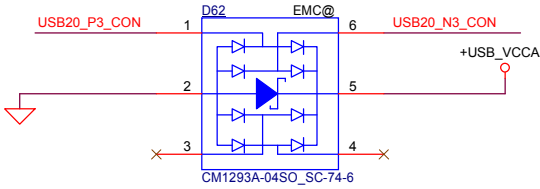
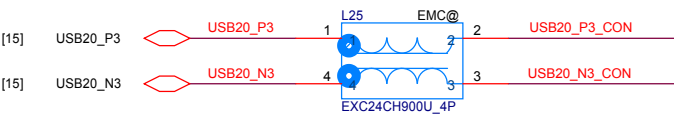
PORT2 (AOU)




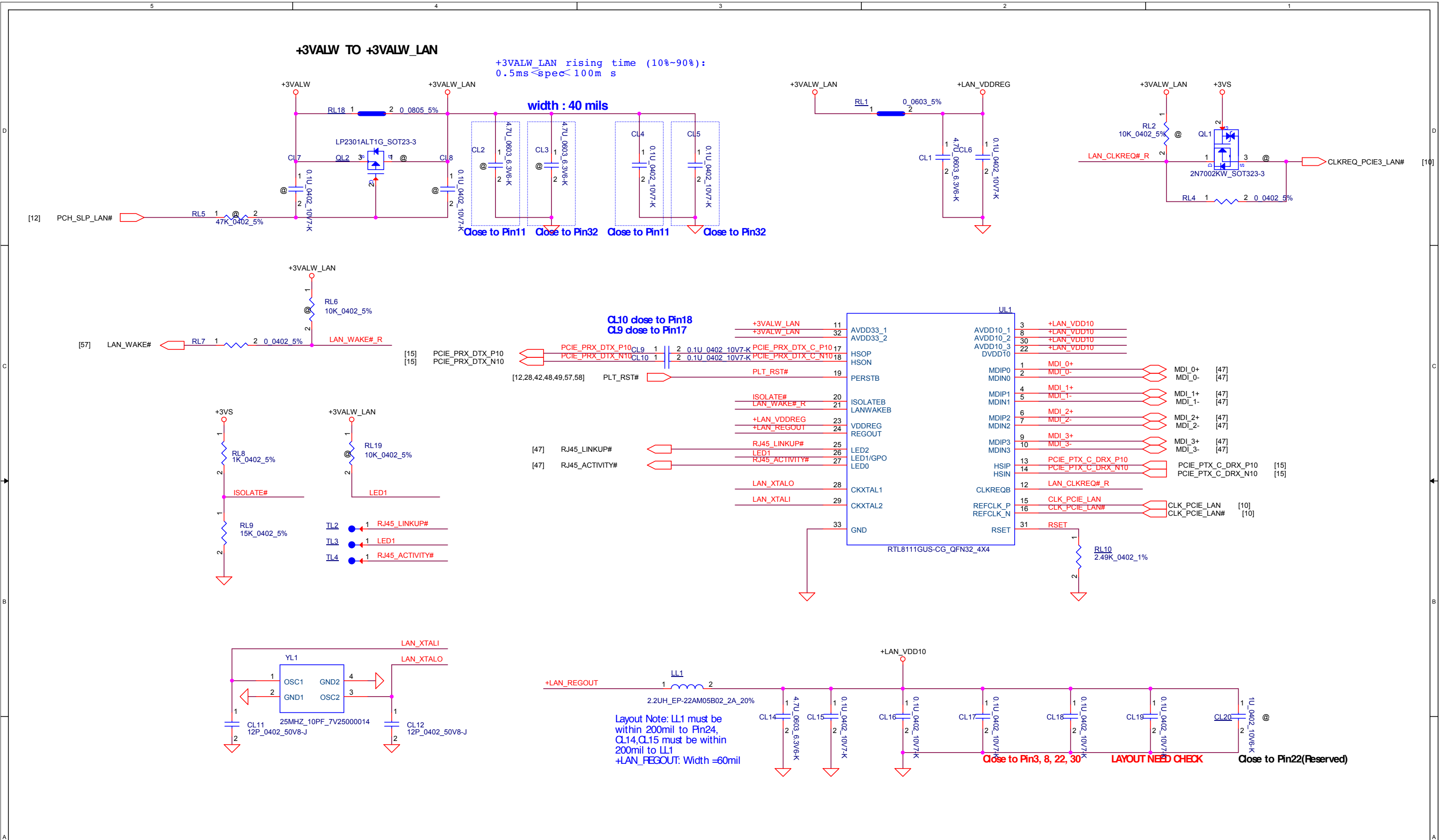
CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

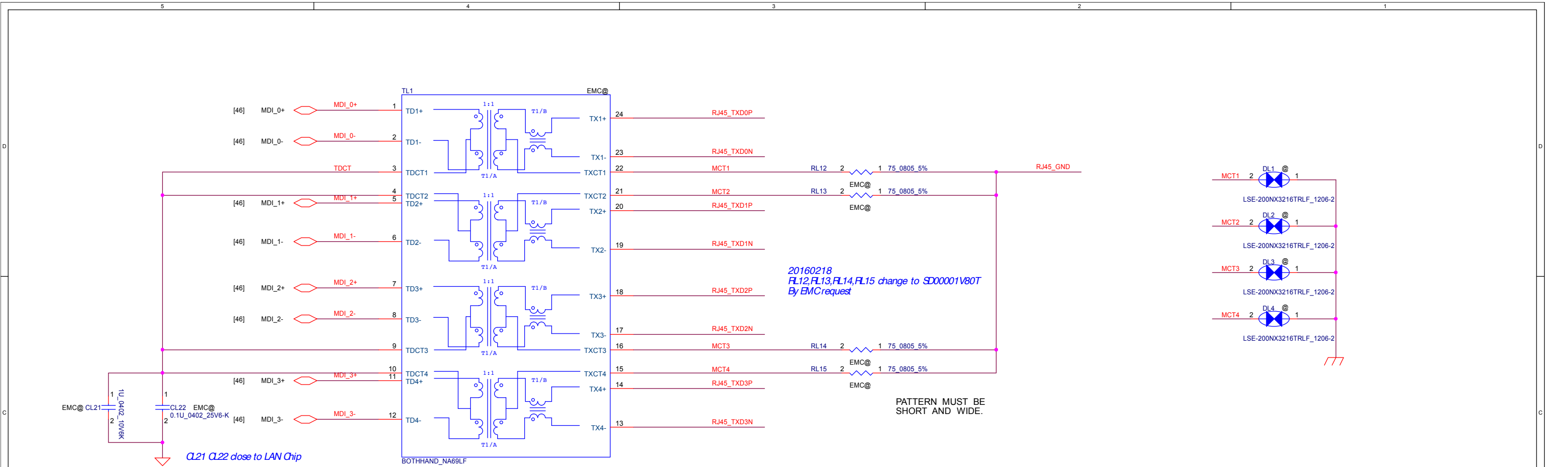


USB3 PORT3

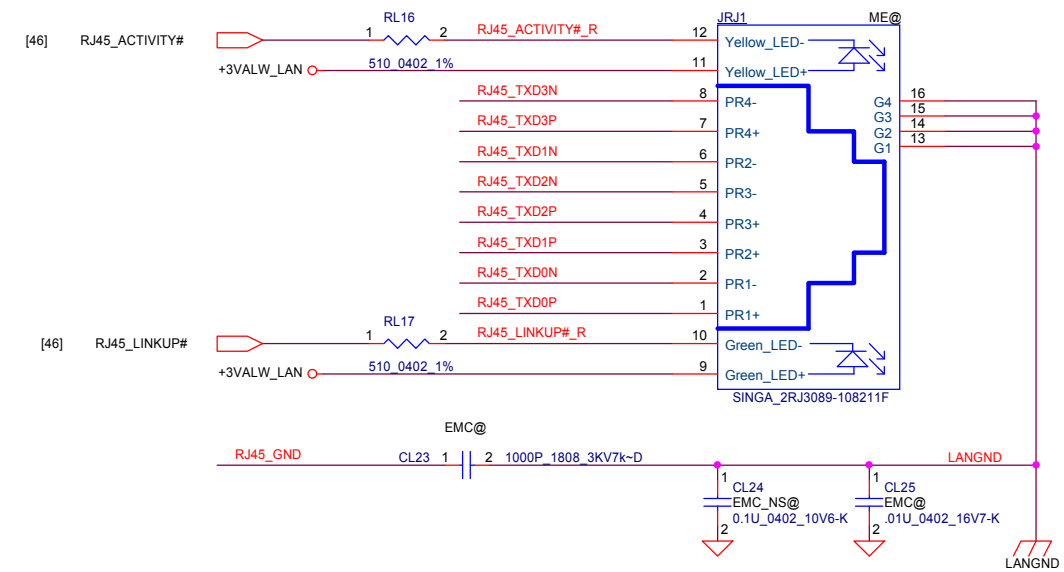
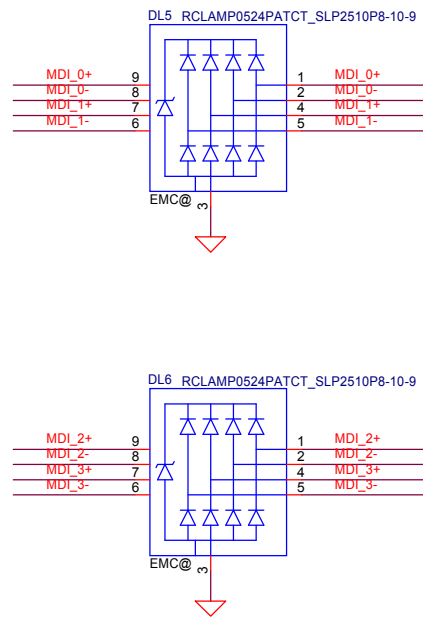


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				Custom	KENOBI	
				Date:	Thursday, August 25, 2016	Sheet 45 of 82

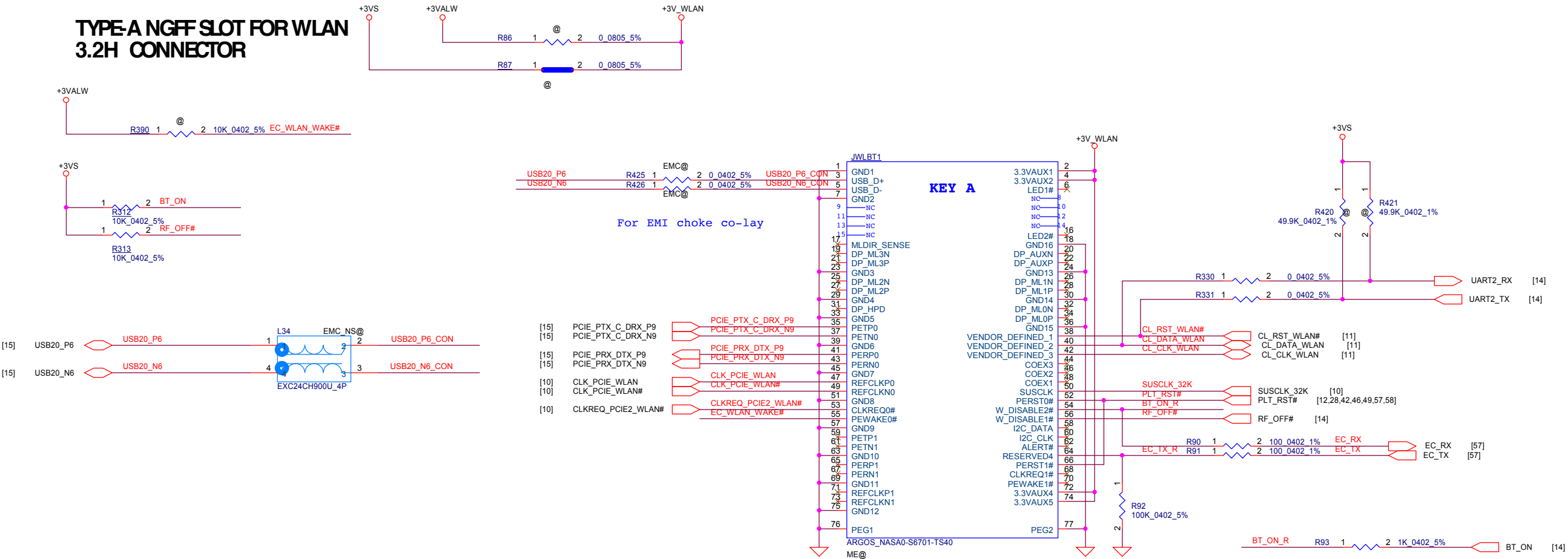


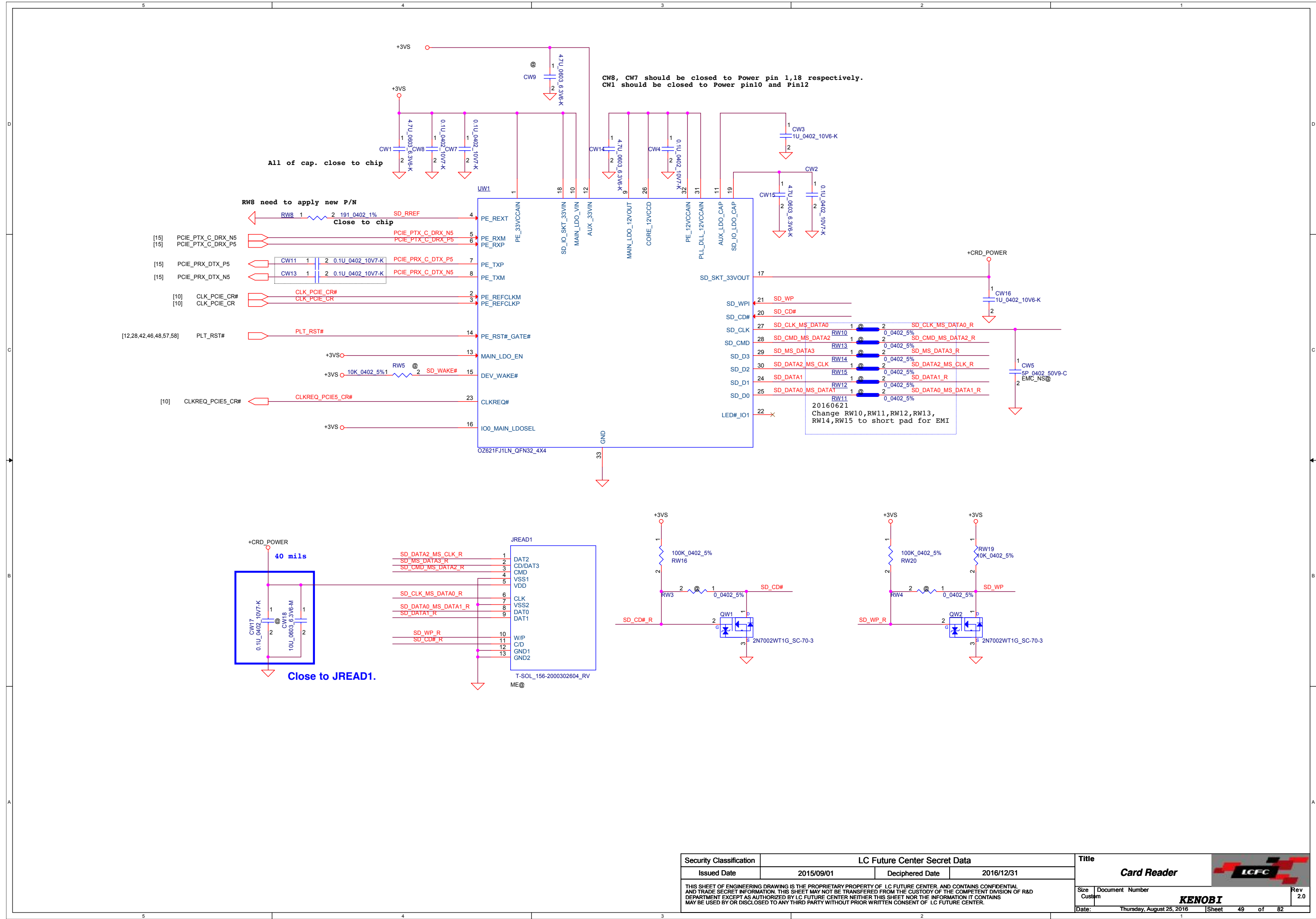


RJ-45 Conn.

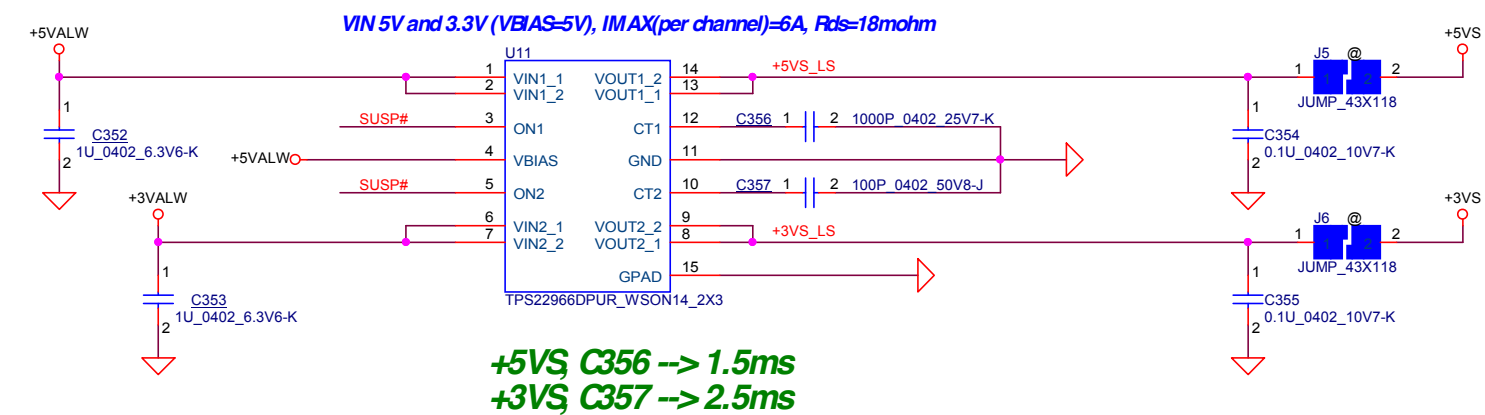


TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR

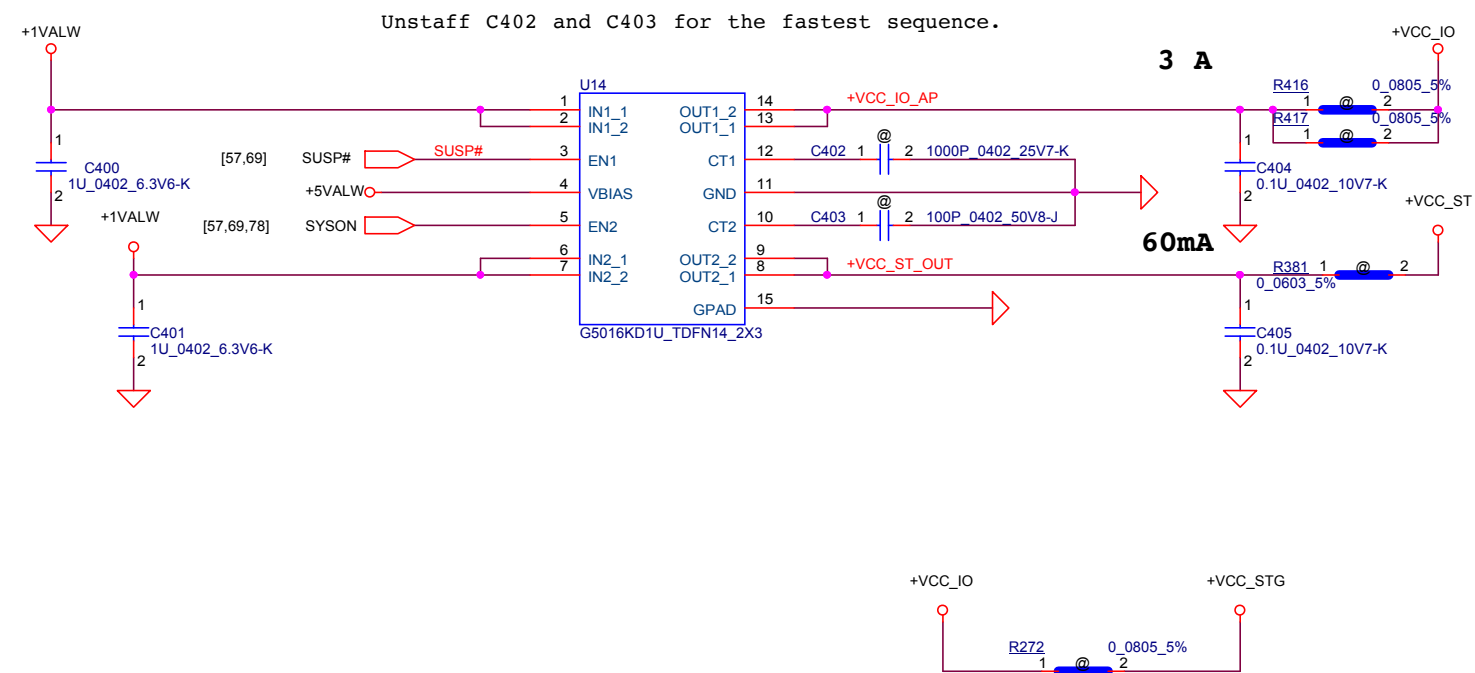




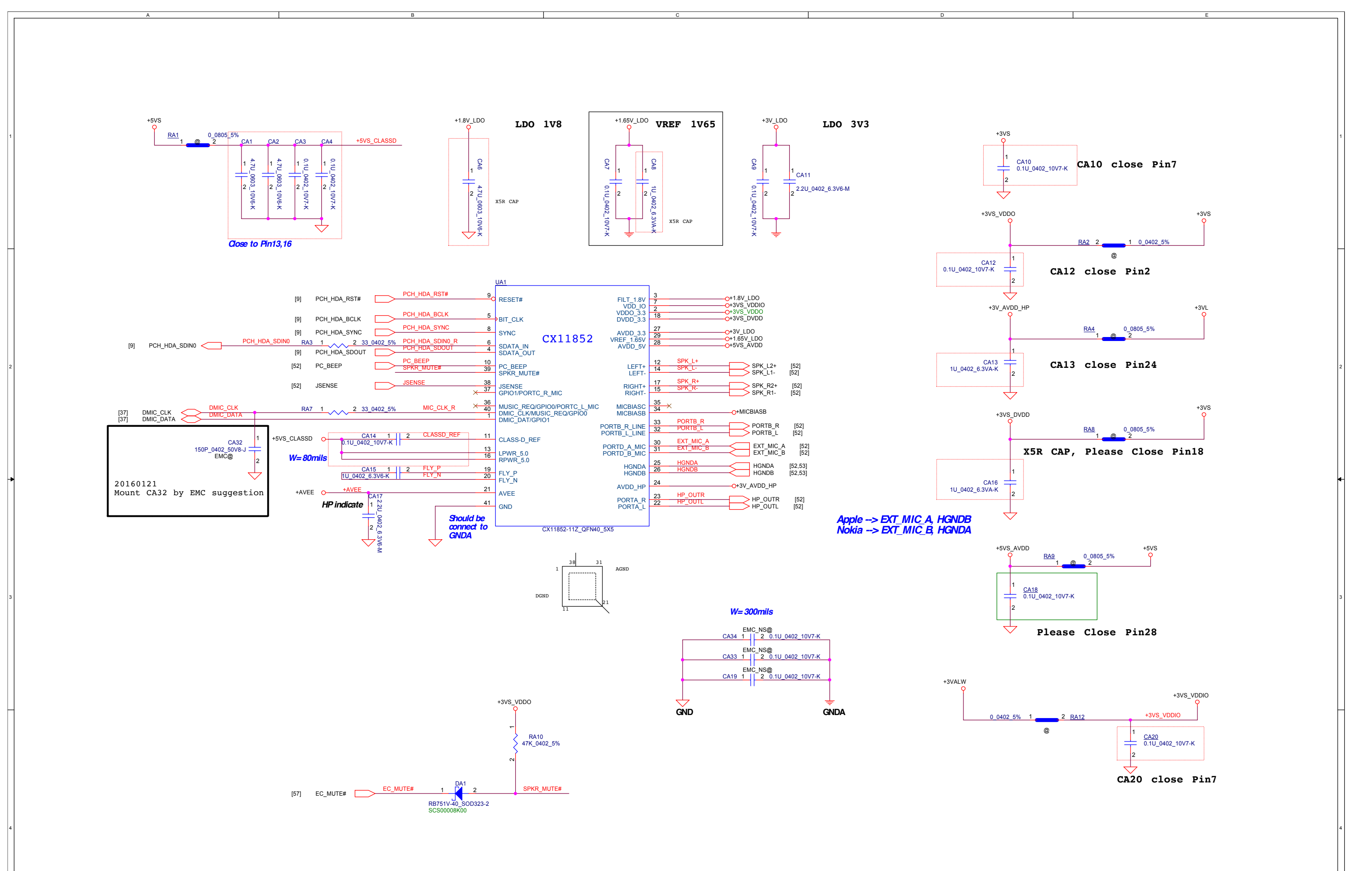
Load Switch
+5VALW To +5VS
+3VALW To +3VS



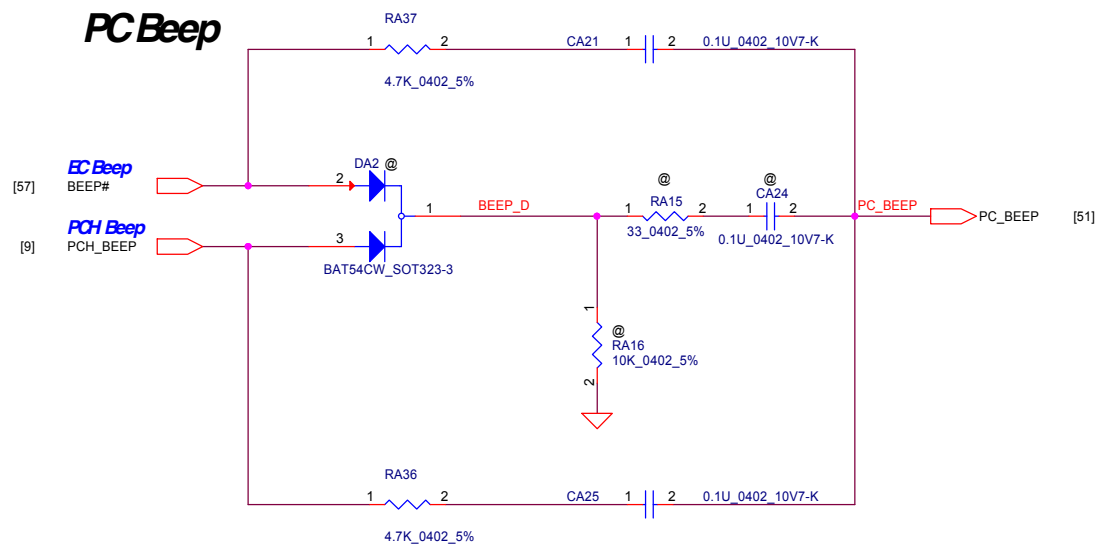
+1VALW to +VCC_IO_AP & +VCC_ST



Slew Rate=10uS<TR<65us

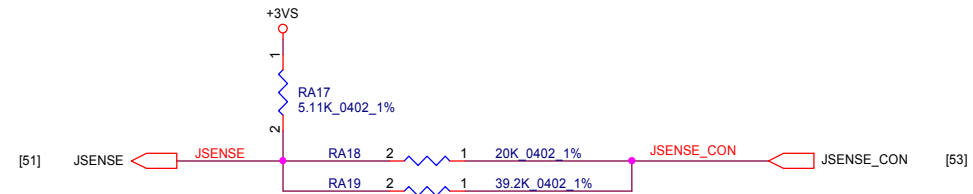
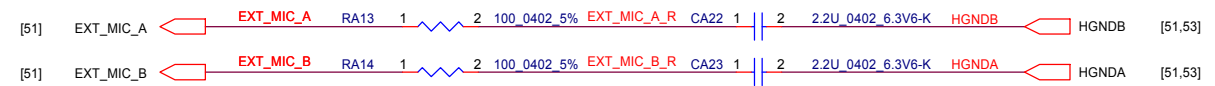


PC Beep

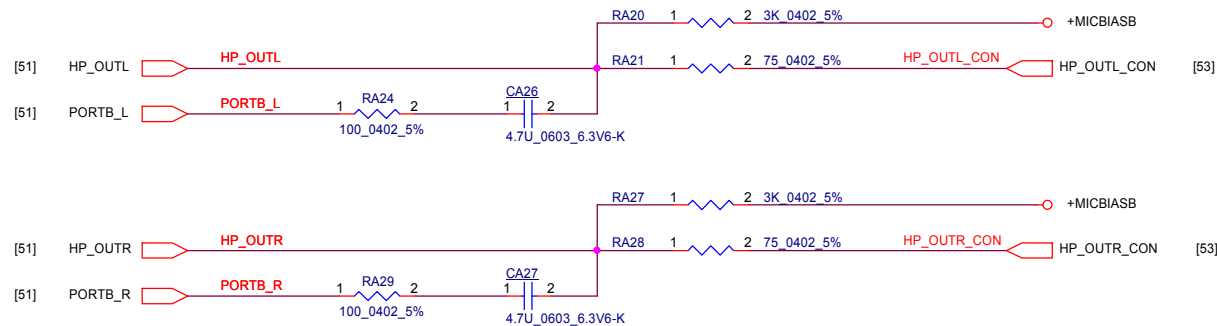


EXT. MIC/LINE IN

Apple -> EXT_MIC_A, HGND B
Nokia -> EXT_MIC_B, HGND A



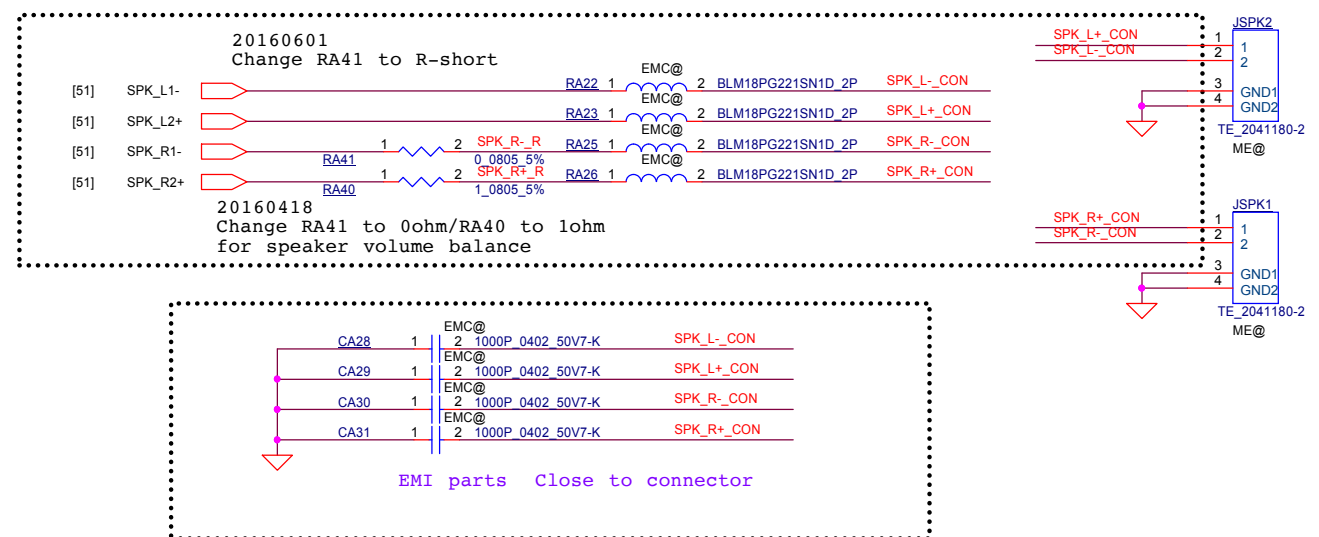
HeadPhone/ LINE OUT




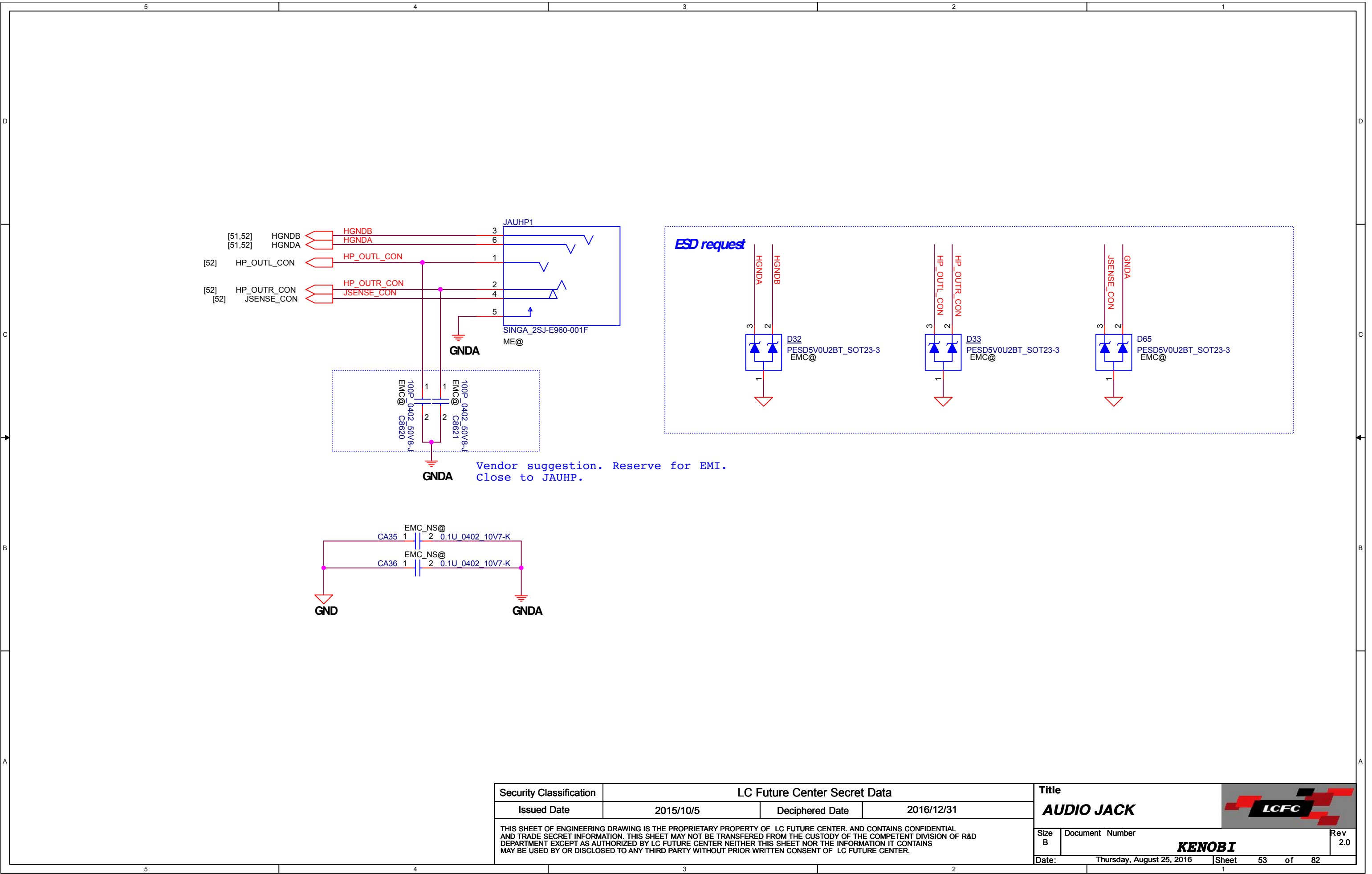
Speaker OUT


Need Lenght Match

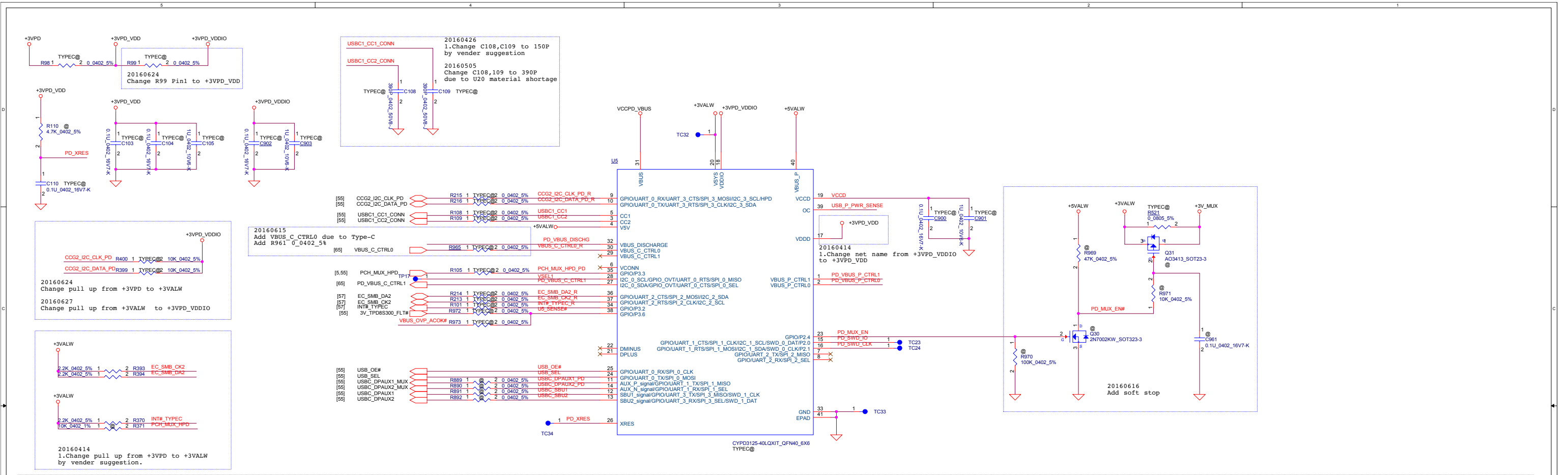
SPK CONN.




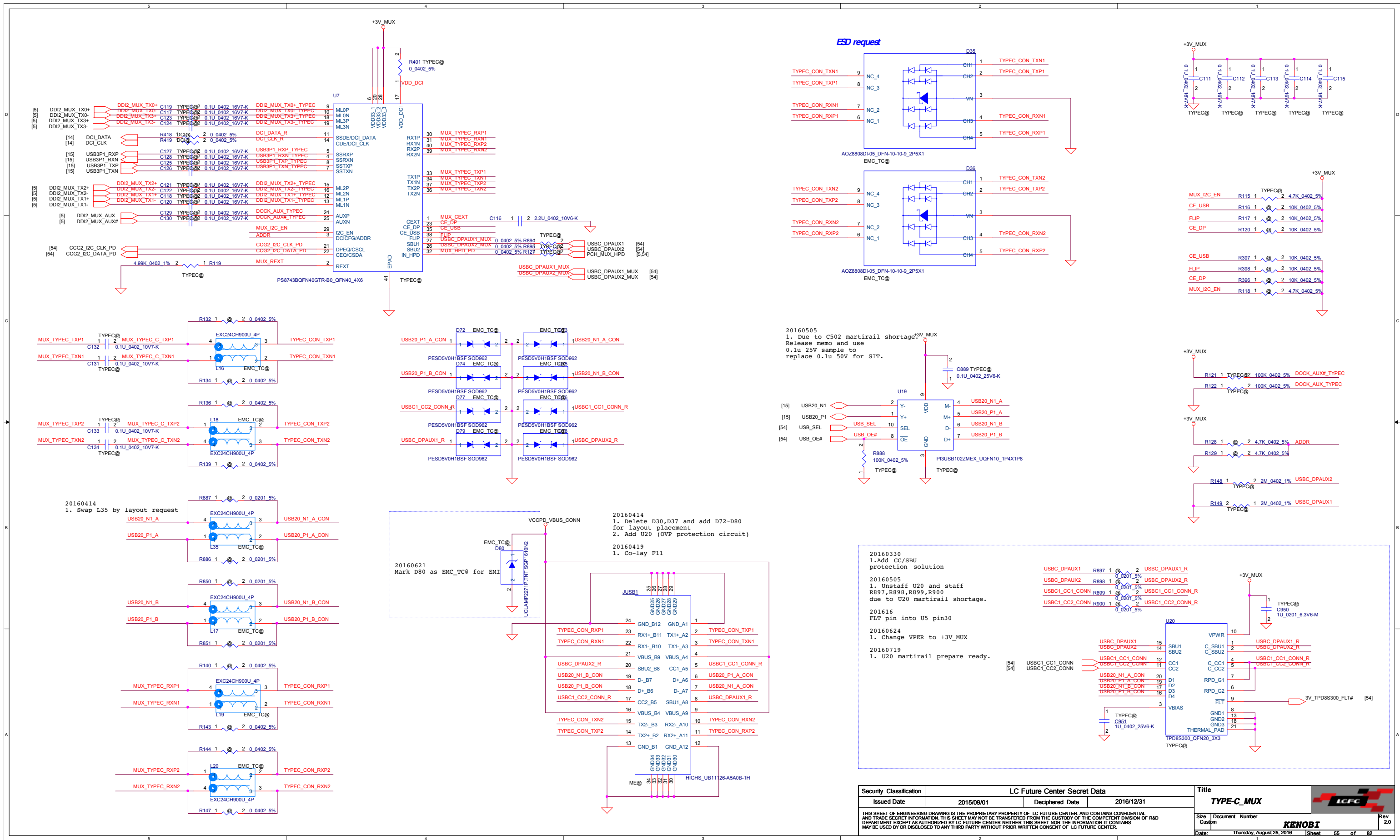
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/09/01	Deciphered Date	2016/12/31	HP/MIC JACK/Speaker		
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				Date:	Thursday, August 25, 2016	Sheet 52 of 82




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Issued Date		2015/10/5	Deciphered Date	2016/12/31			AUDIO JACK			
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Date:		Thursday, August 25, 2016			Sheet	53	of	82	Rev	2.0



<p>Security Classification</p> <p>Issued Date</p> <p>Deciphered Date</p> <p>2015/09/01</p> <p>2016/12/31</p>		<p>LC Future Center Secret Data</p>		<p>Title</p> <p>TYPE-C_Controller</p>		
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>						
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Custom				2.0		
Date		Thursday, August 25, 2016		Sheet 54 of 82		



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Issued Date	2015/09/01	Deciphered Date	2016/12/31	TYPE-C_MUX 	
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				Date: Thursday, August 25, 2016	Sheet 55 of 82

Blank drawing area.

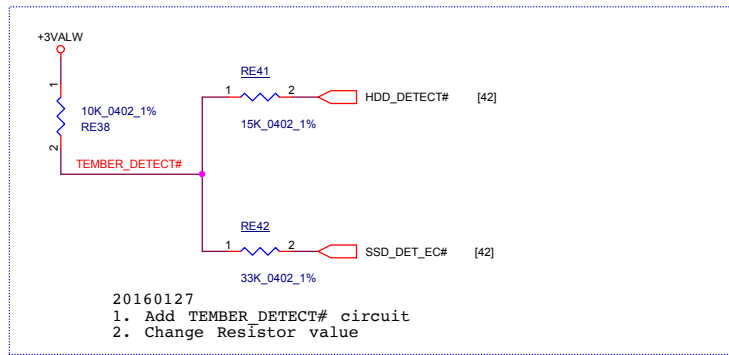
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Security Classification	LC Future Center Secret Data			
Issued Date	2015/10/5	Deciphered Date	2016/12/31	

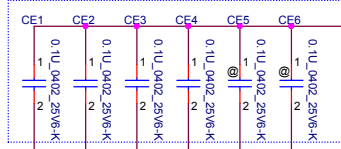
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Custom	KENOBI	2.0

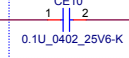
Date:	Thursday, August 25, 2016	Sheet	56	of	82
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All capacitors close to EC



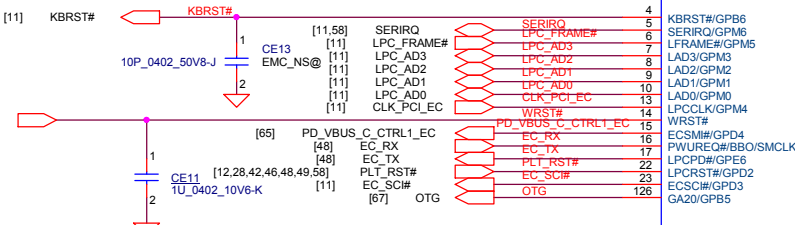
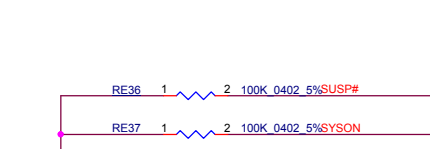
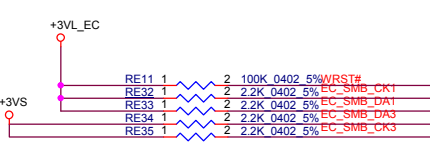
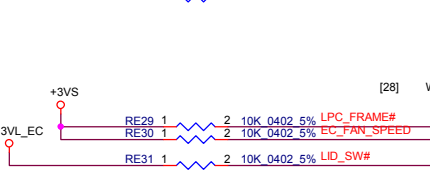
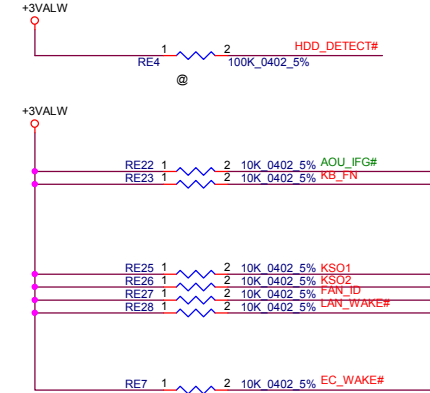
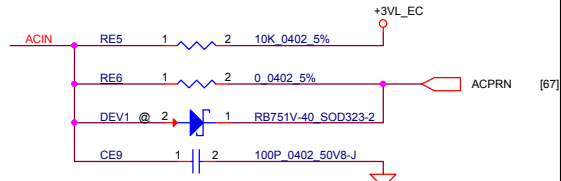
Close to EC



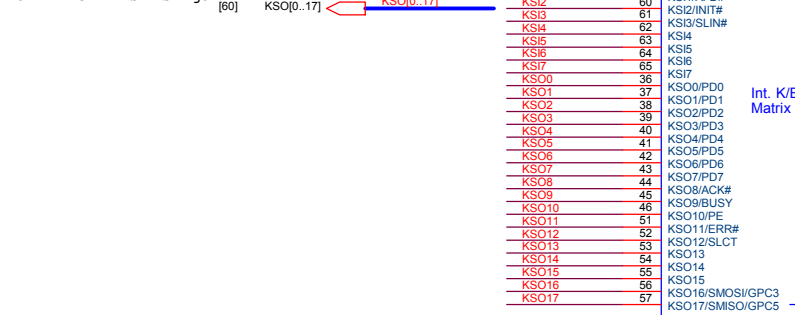
minimum trace width 12 mil

Vcc		3.3V +/- 5%			
RE1		100K +/- 1%			
Board ID	RE2	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	OK +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

20160419
Change RE2 to 18K
for SIT board ID



20160307
Stuff CE11 for WRST signal



IT8586E/AX
LQFP-128L

EXTERNAL SERIAL FLASH

SPI Flash ROM

UART

GPIO

GPIO

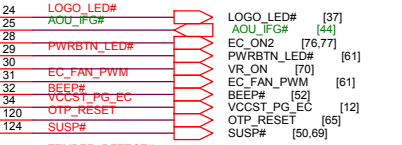
GPIO

GPIO

GPIO

GPIO

GPIO



ADC

DAC

PS2

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

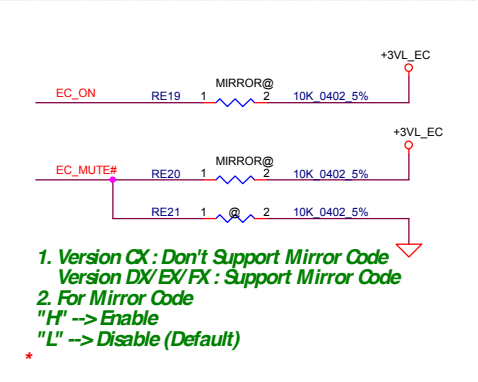
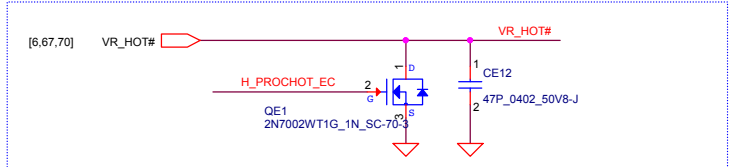
GPIO

GPIO

GPIO

Please don't place any PU Resistor on GPG[7:2]
(Reserve hardware strapping)

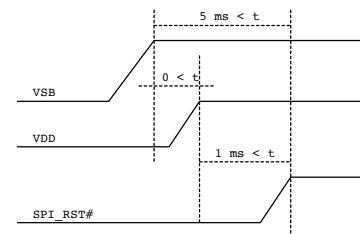
Un-stuff if not necessary.



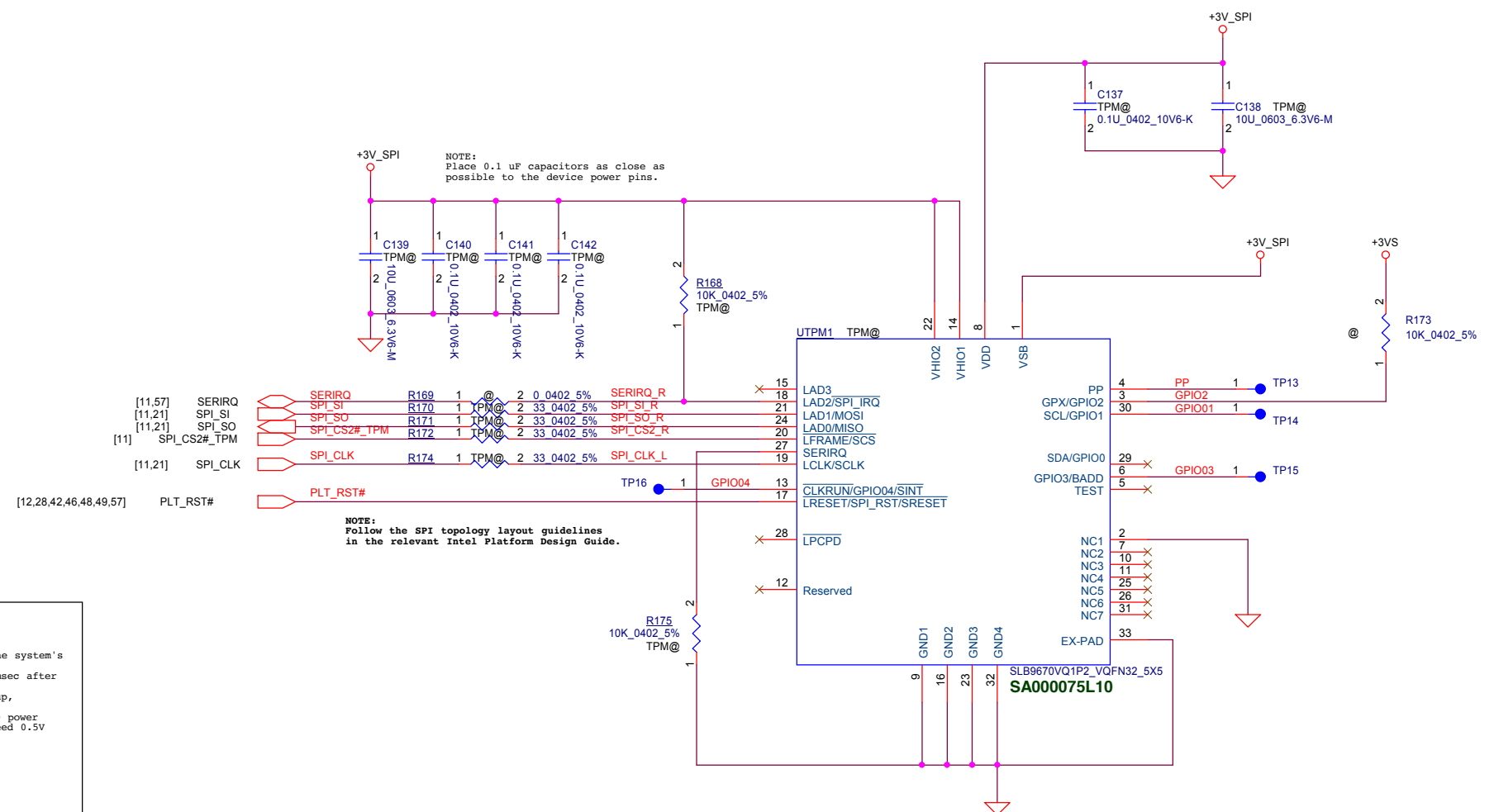
Pin No	TCG PTP Signal (x30)	Infinion SLB91YWQ1.2 FW 1.10	ST Micro ST32H7PM2E32AA09	Navtecs NFC7E53LB0YX
1	VDD	VDD	NC	VSS
2	GND	GND	GND	NC
3	GPIO	NC	NC	GP2/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	CPH0	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DMC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MCOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DMC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

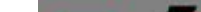
Follow THP1_SWG_SIT_EC005, update TPM table

NOTE:
Check timing sequence in SDV phase.

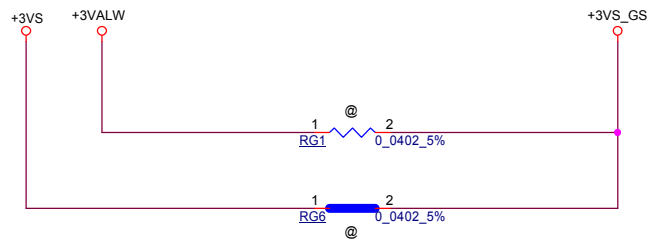


- NOTE:
- 1) It is recommended to connect the TFM to the system's standby voltage to improve performance.
 - 2) SPI RST# must be asserted for at least 5 msec after VSB power-up.
 - 3) VSB may come up anytime before VDD power-up, but not after VDD power-up.
 - 4) SPI RST# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.



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				Date: Thursday, August 25, 2016		Sheet 58 of 82	





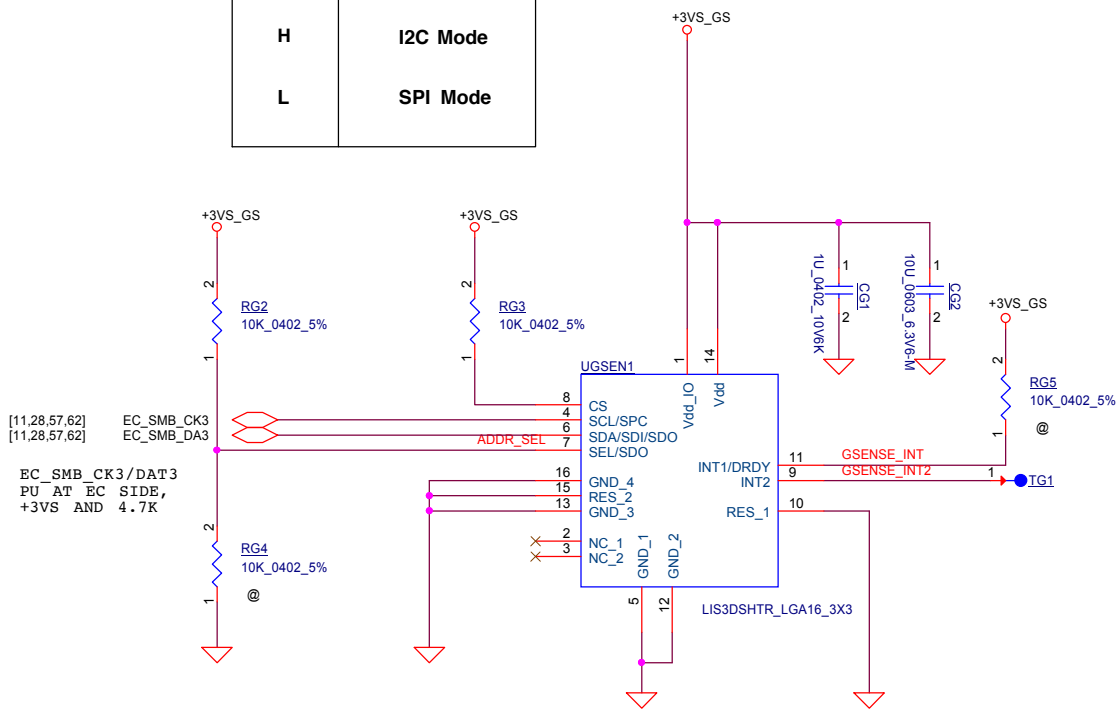
APSG-Sensor

TABLE

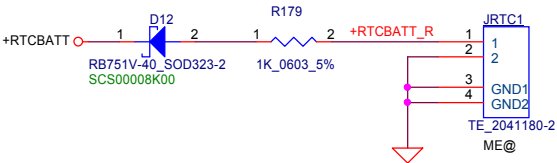
P/N	ADDR_SEL	Address
LIS3DSHTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE

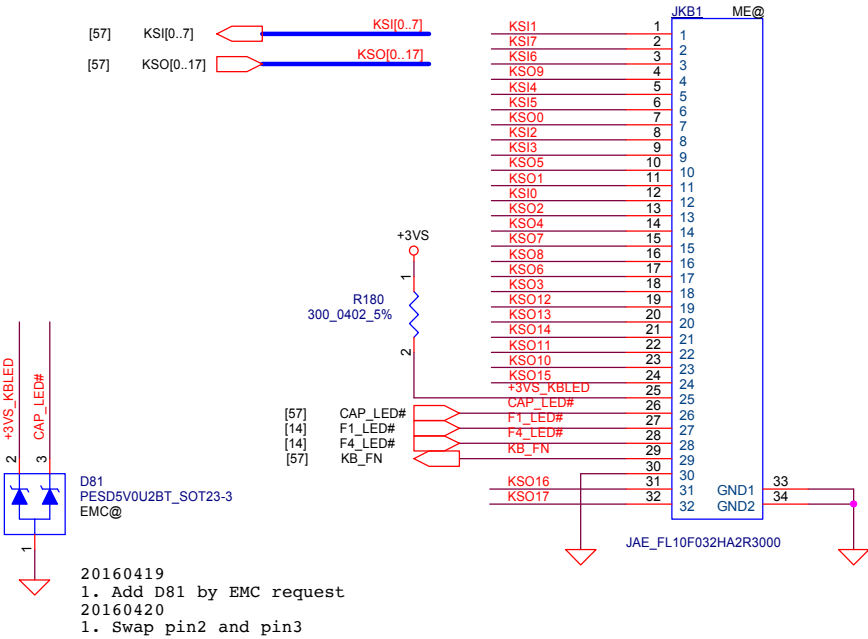
P/N	Mode Selection
H	I2C Mode
L	SPI Mode



RTC CONN.

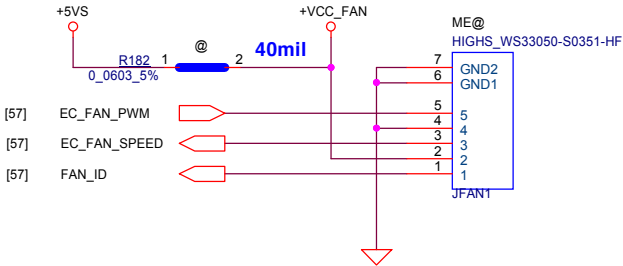


KB CONN

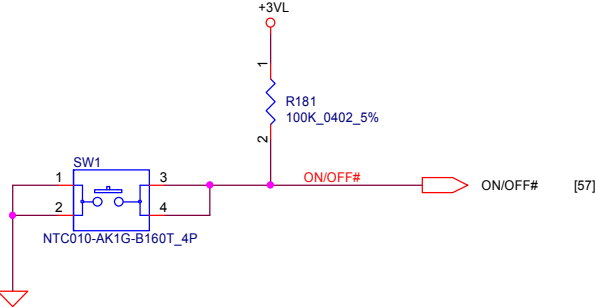
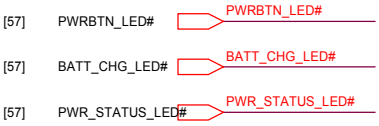
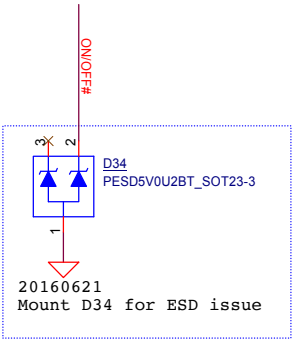
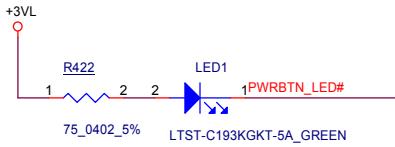
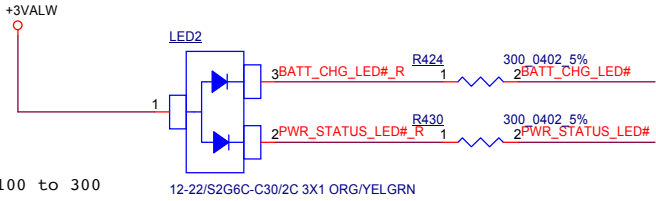


20160419
1. Add D81 by EMC request
20160420
1. Swap pin2 and pin3

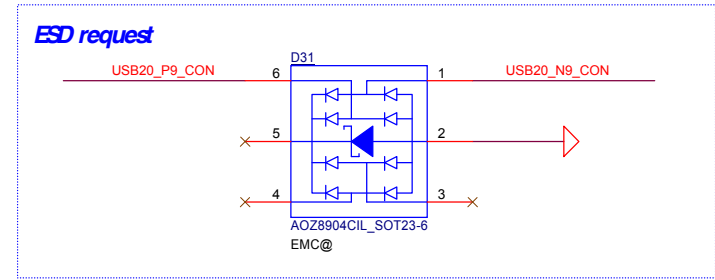
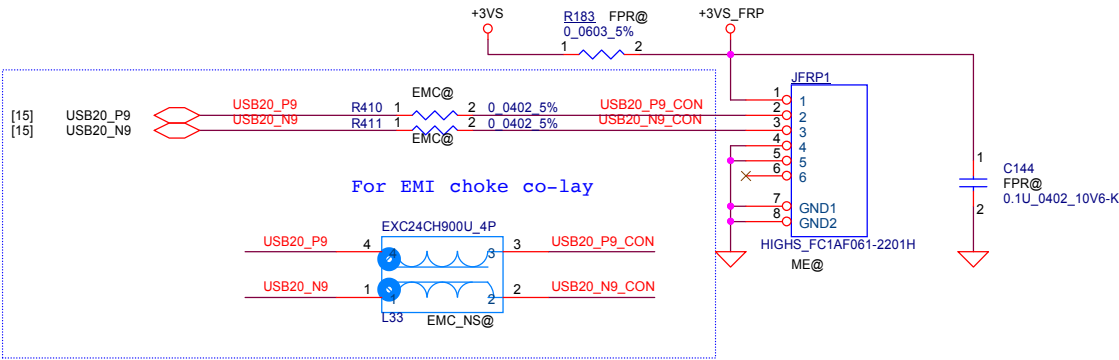
FAN CONN.



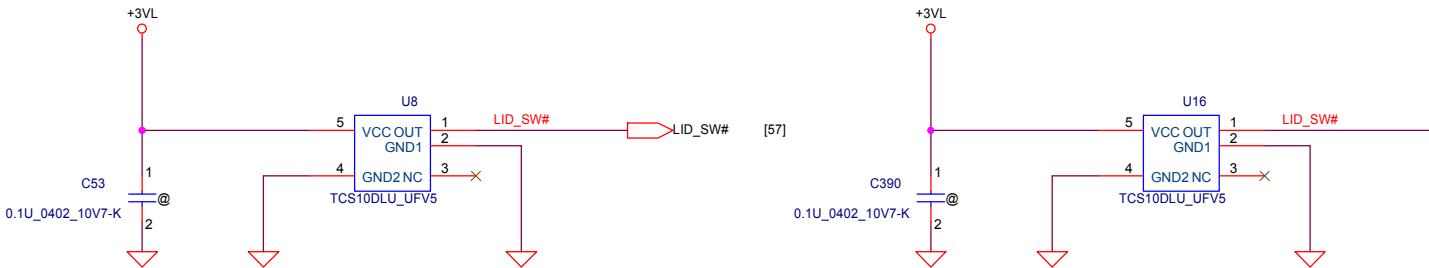
20160424
1. Change R430/R423 from 100 to 300 ohm for LED brightness
2. Change R422 from 100 to 75 ohm for LED brightness



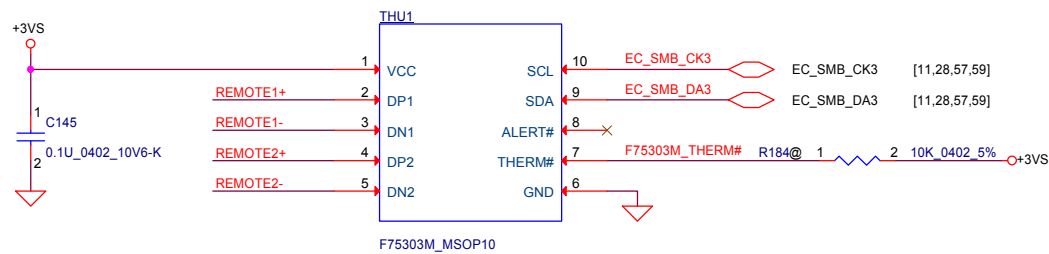
FingerPrint CONN.



Lid Switch

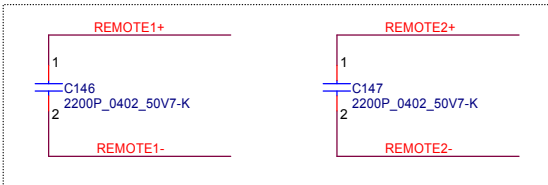


Thermal Sensor
placed near by VRAM

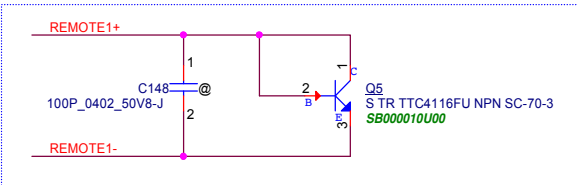


Address 1001_101xb
Internal pull up 1.2K to 1.5V
R for init i d t h e r m a l shut down t e m p

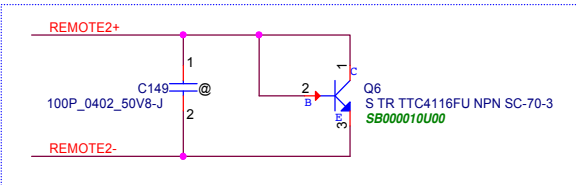
Close to U1



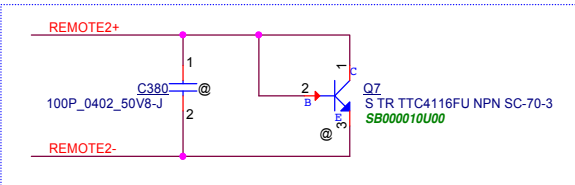
Close to +VCC CORE

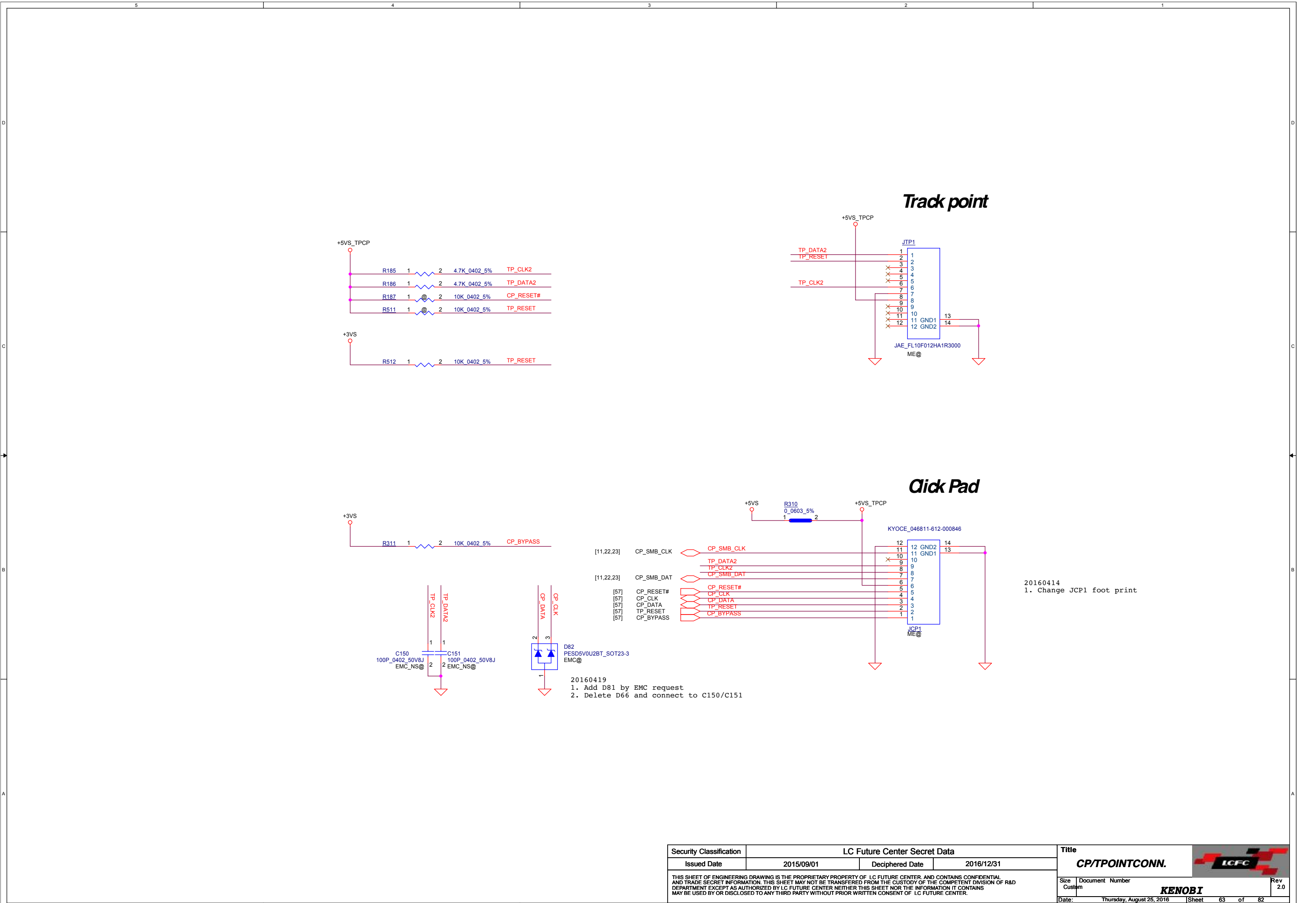


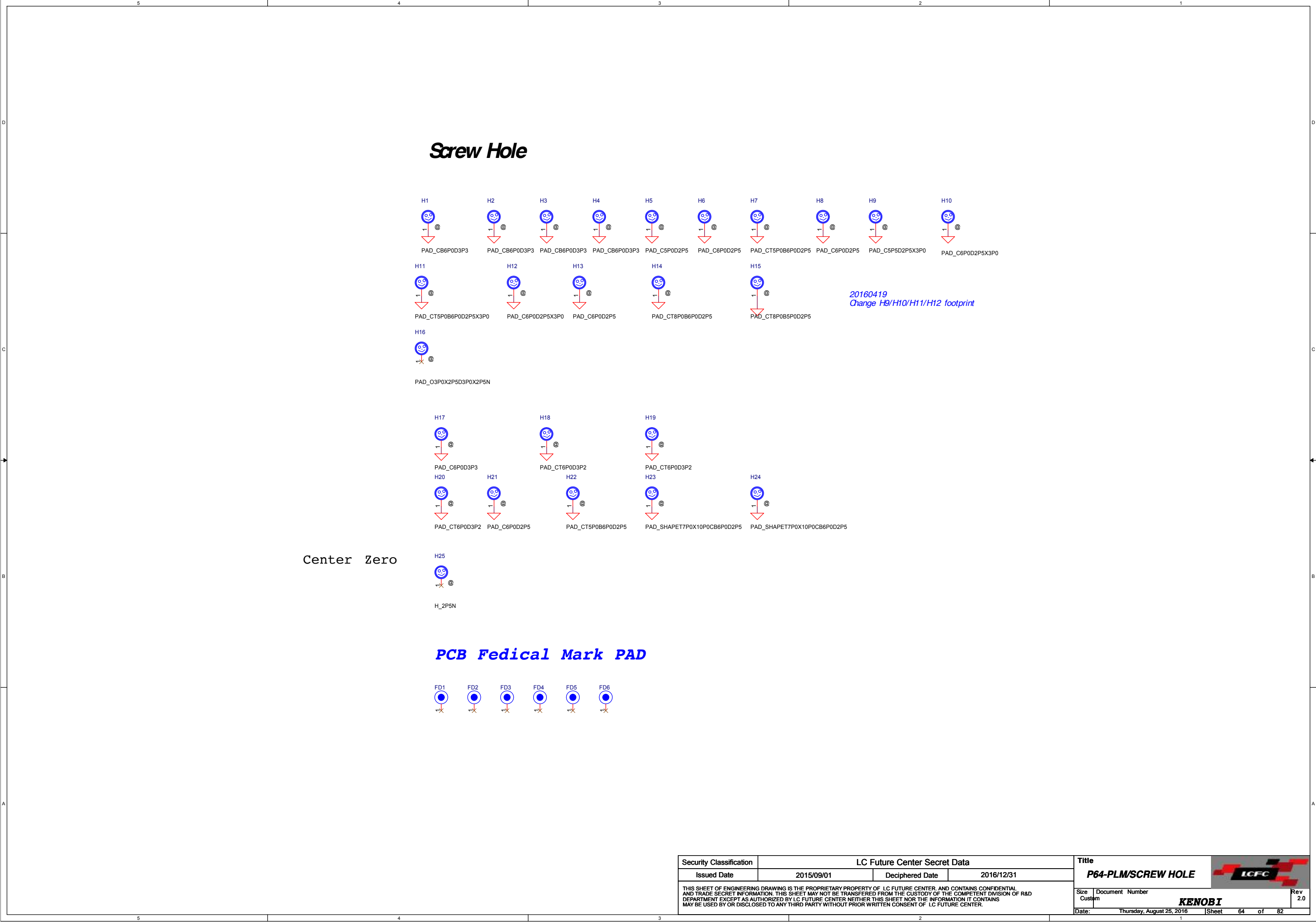
Close DIMM1&.DIMM2

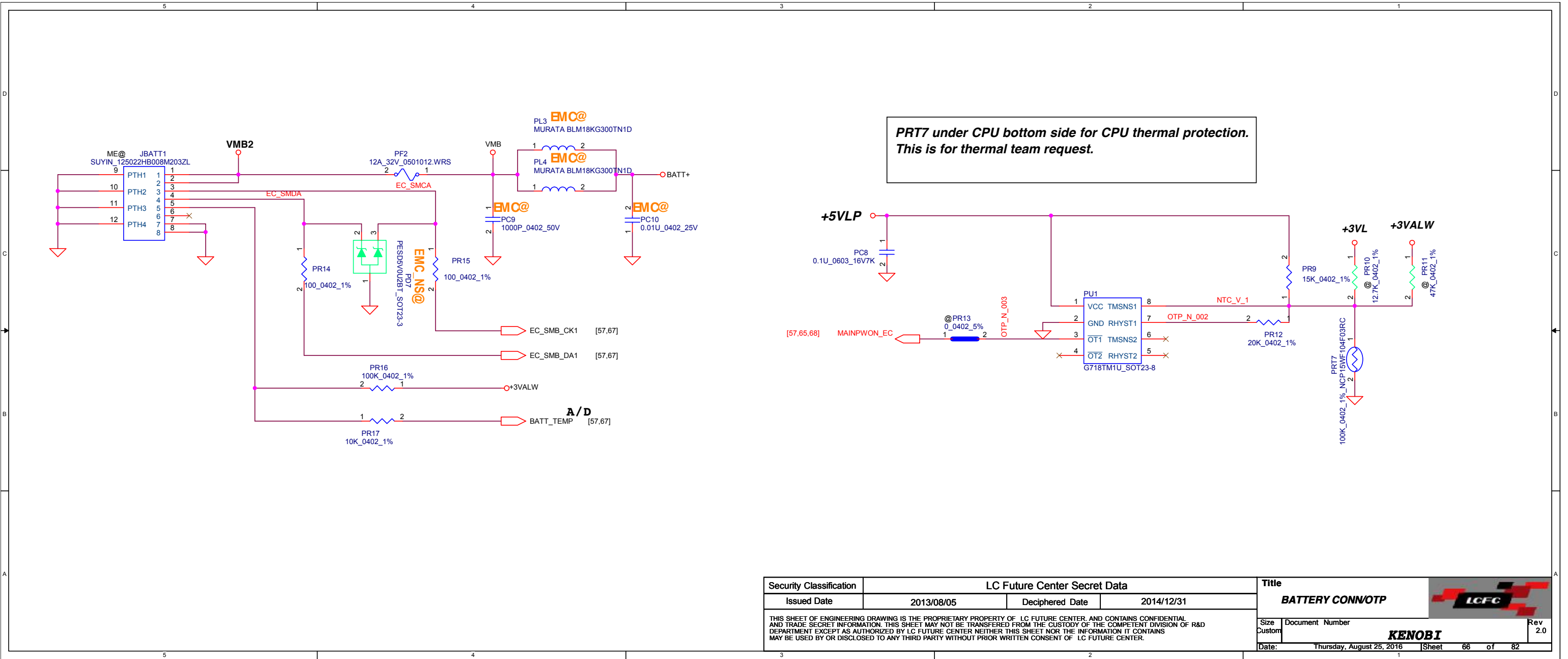


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

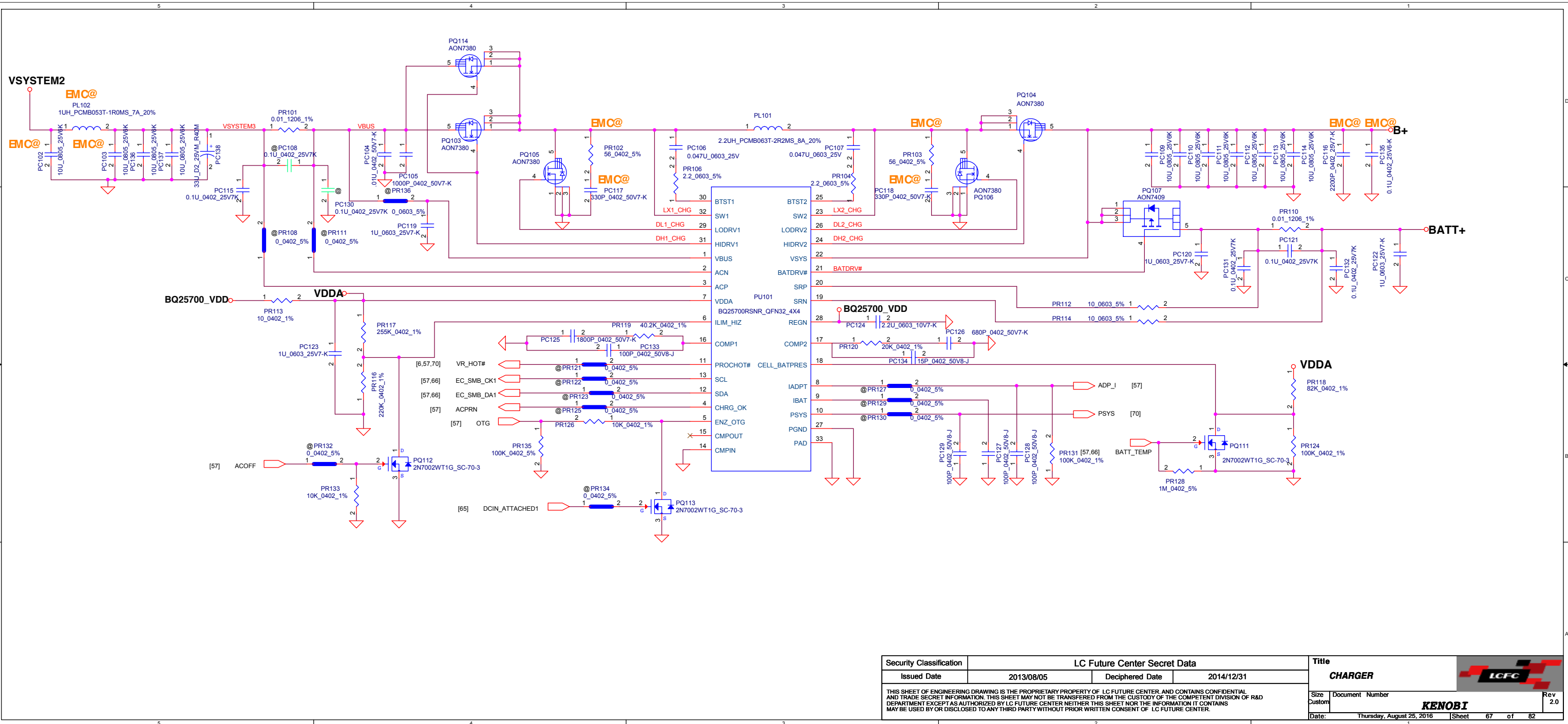


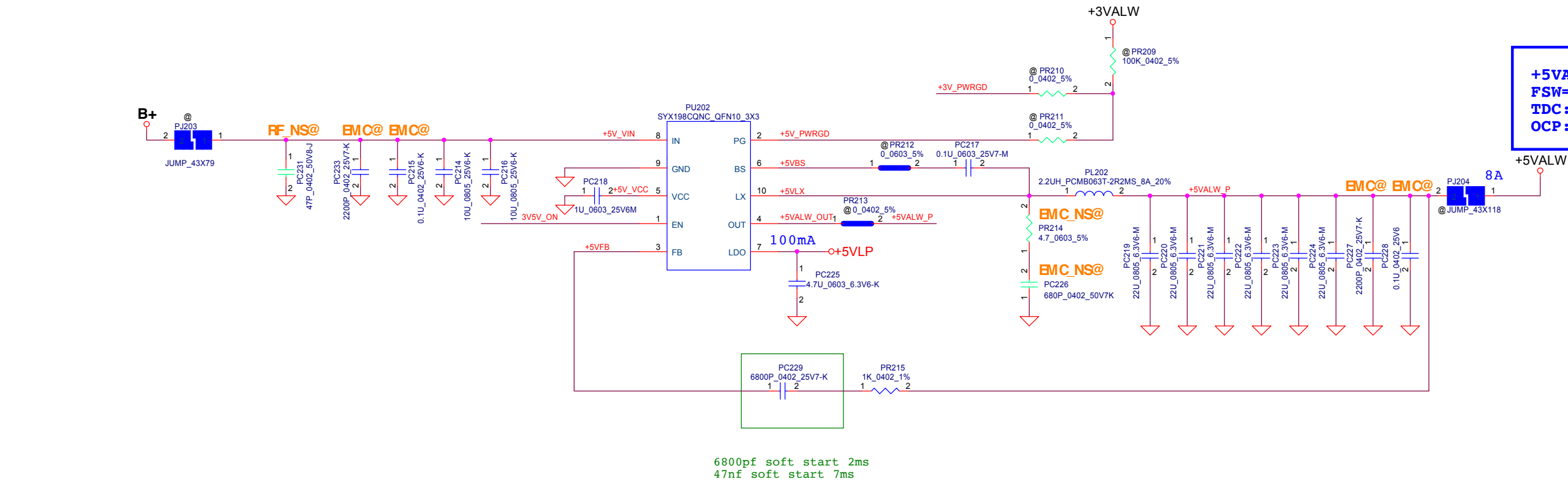
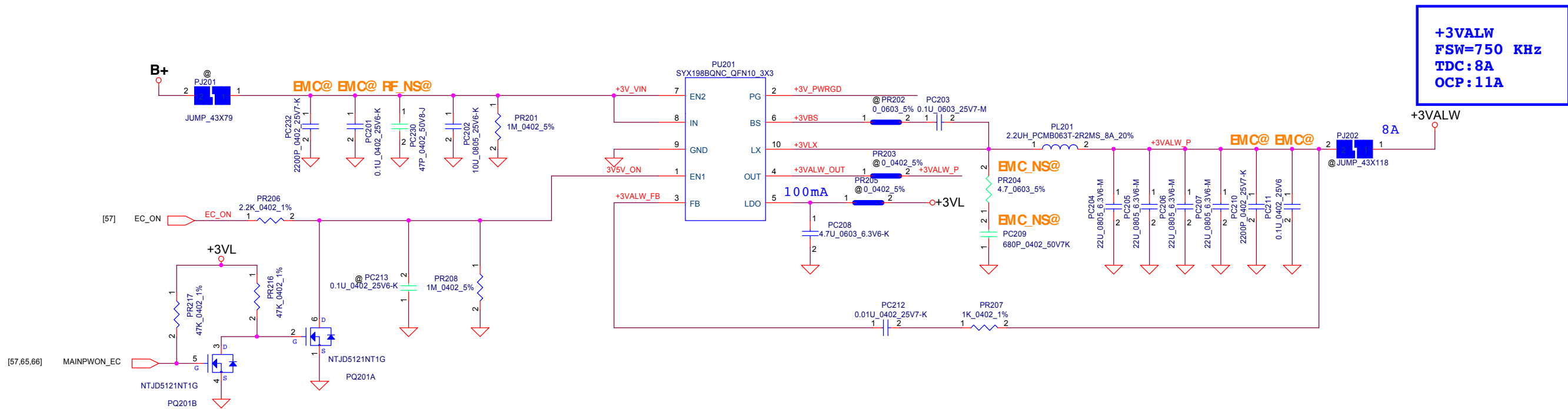





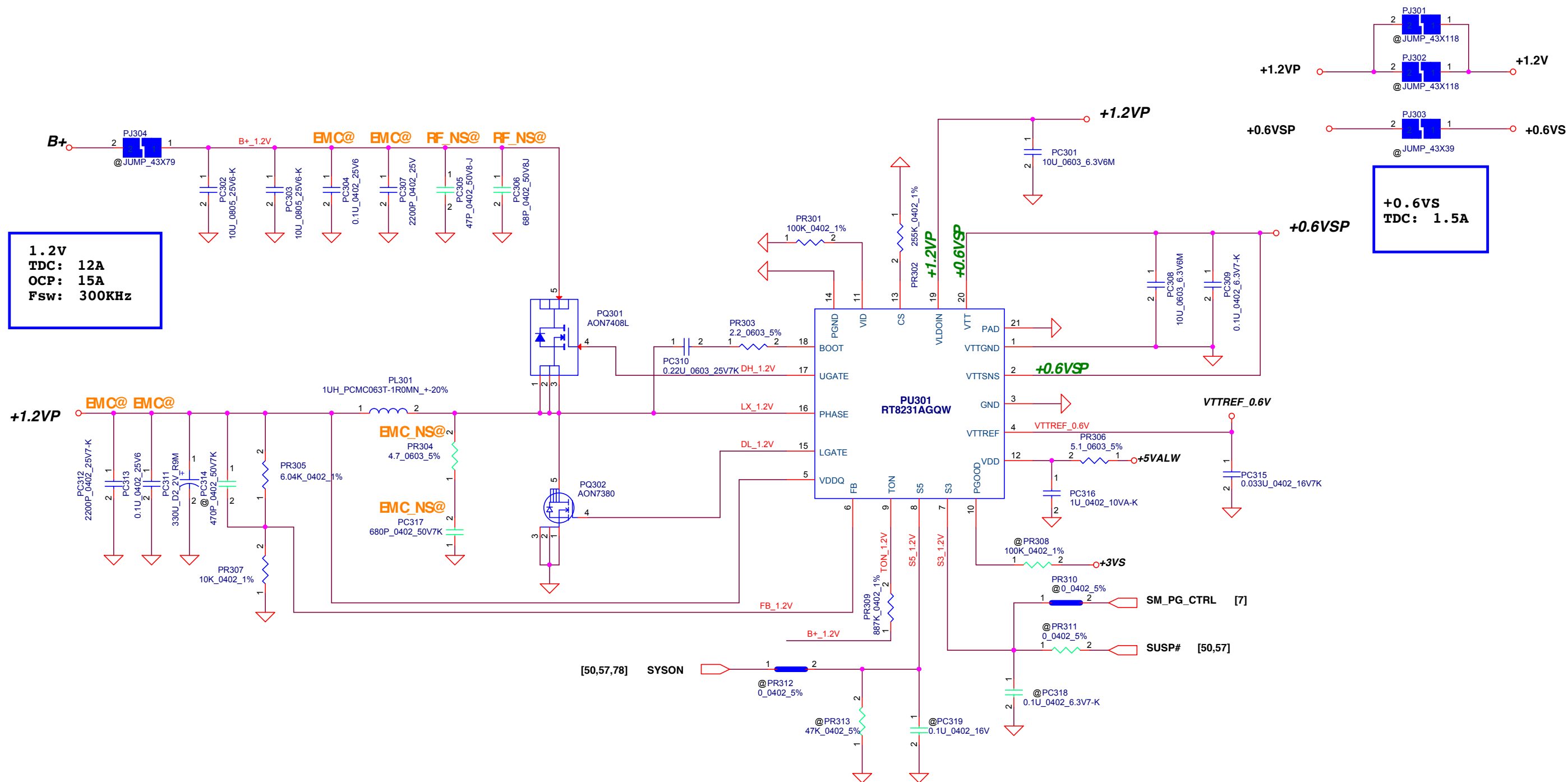


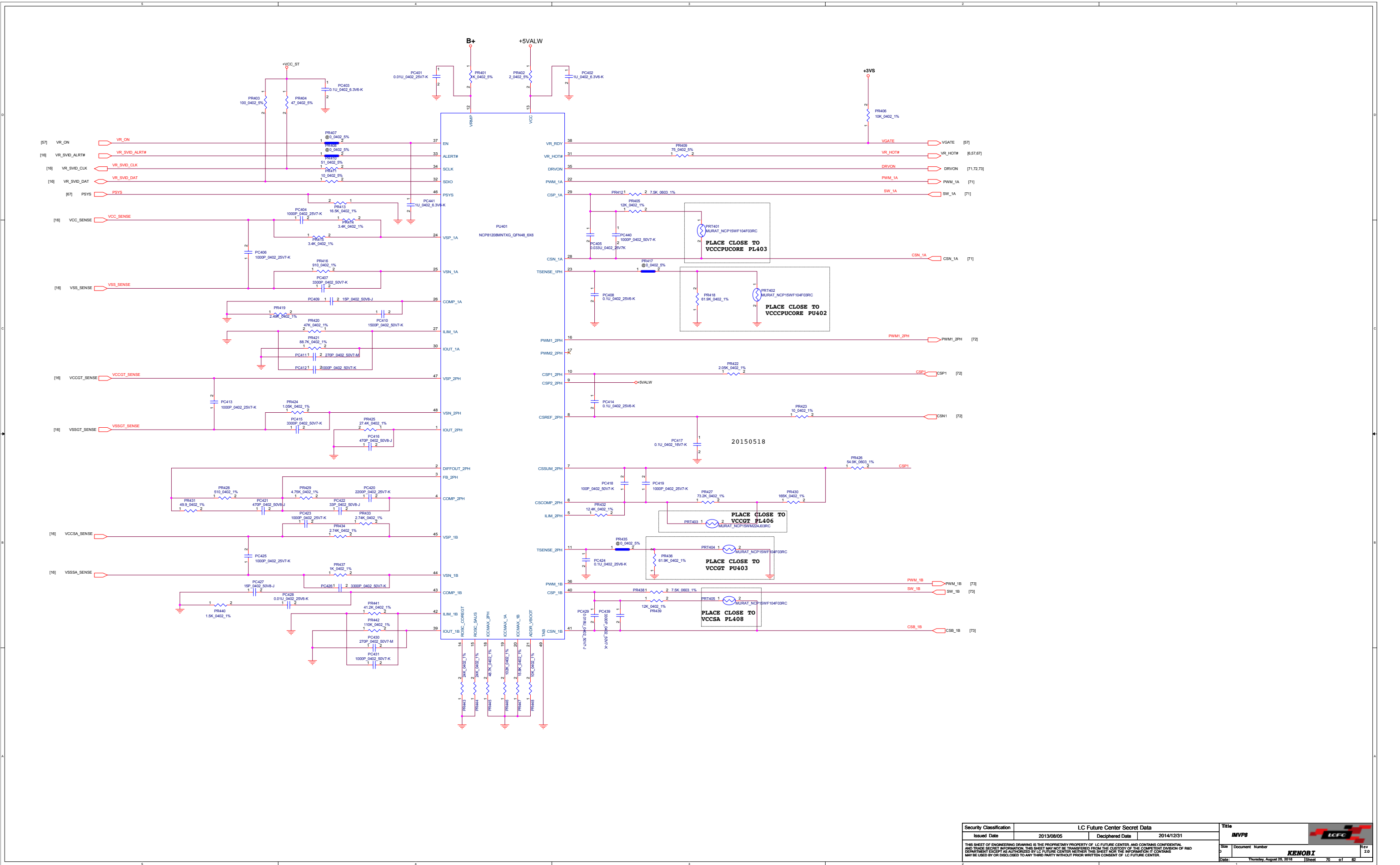
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/05	Deciphered Date	2014/12/31	BATTERY CONN/OTP	
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				Date: Thursday, August 25, 2016	Rev 2.0
				Sheet 66	of 82

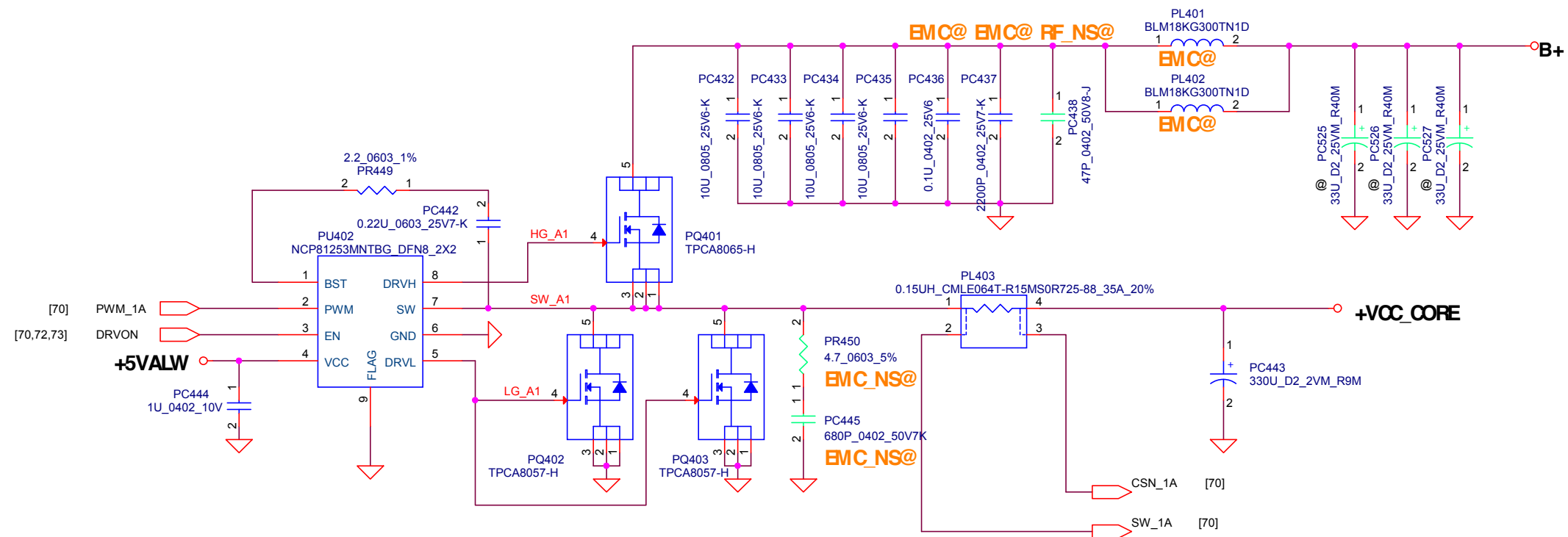





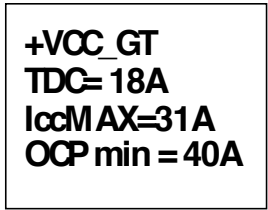
Security Classification		LC Future Center Secret Data				Title							
Issued Date		2013/08/08		Deciphered Date		2013/08/05				3VALWP/5VALWP			
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										KENOBI			
								Date: Thursday, August 25, 2016		Sheet 68 of 82			




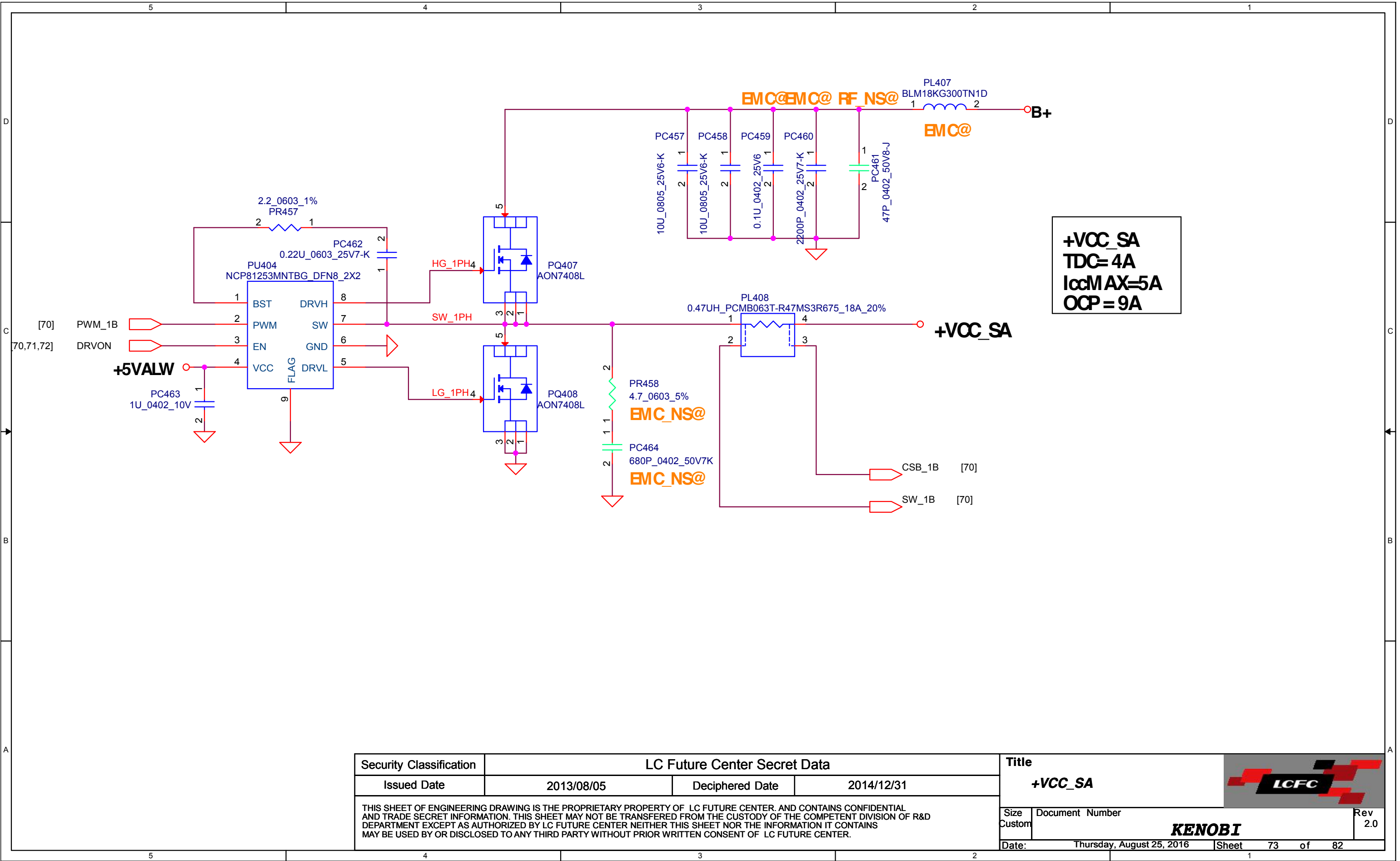


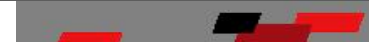


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Issued Date	2013/08/05	Deciphered Date	2014/12/31	+VCC_CORE		
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				Date:	Thursday, August 25, 2016	Sheet 71 of 82

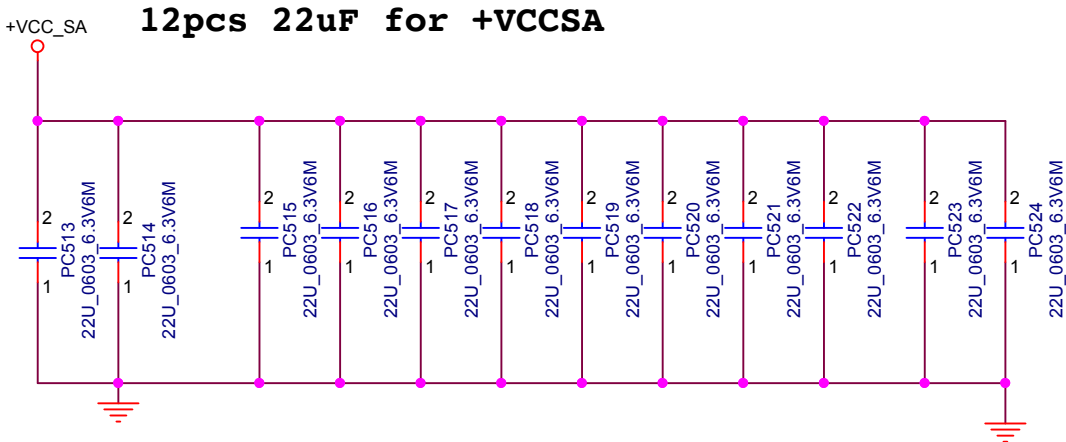
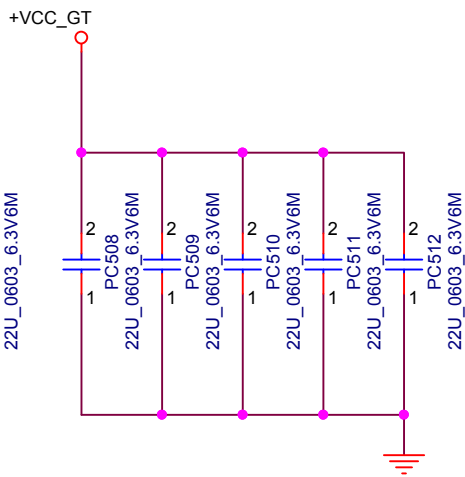
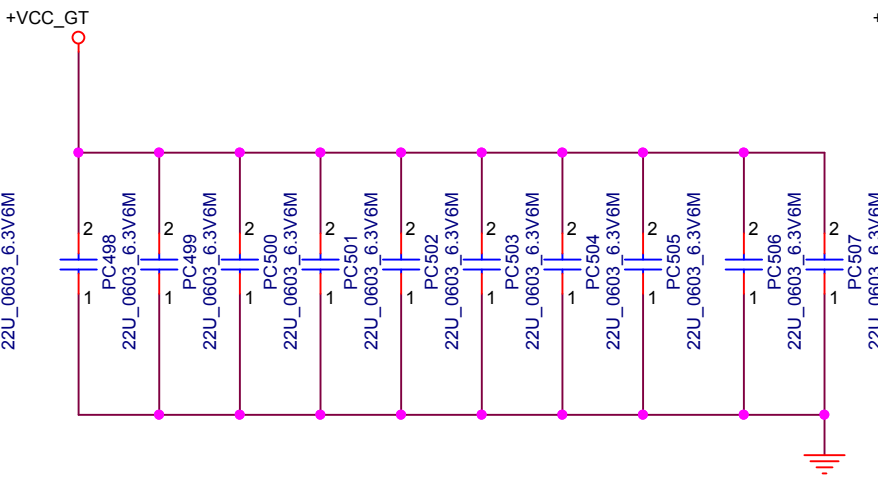
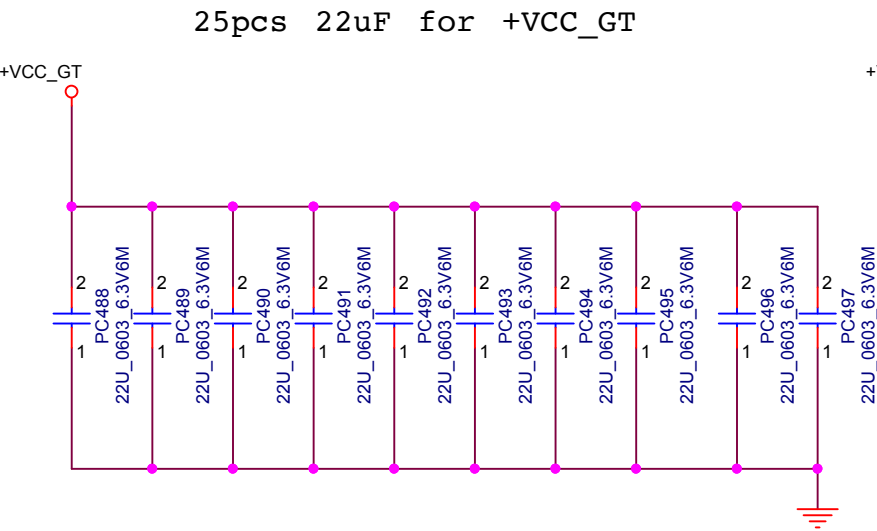
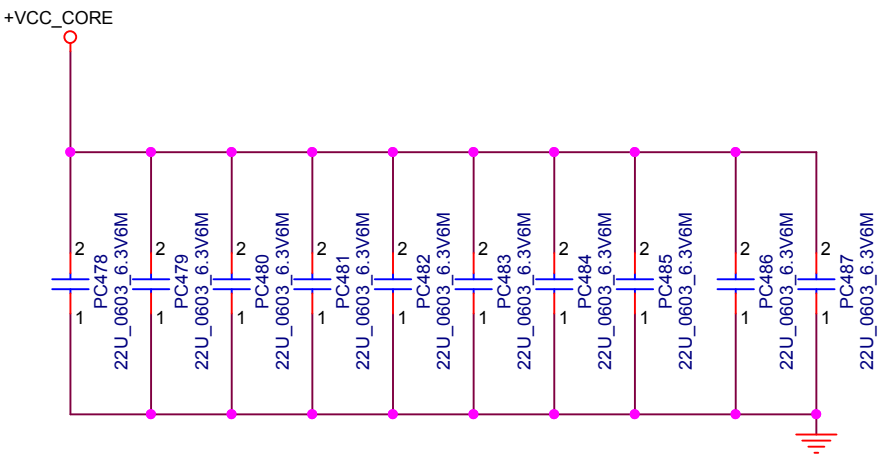
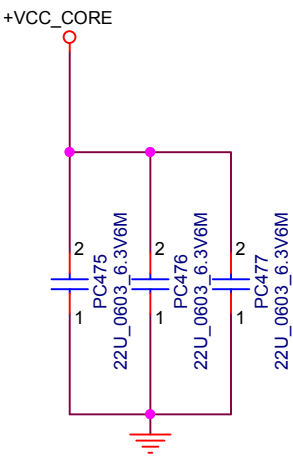
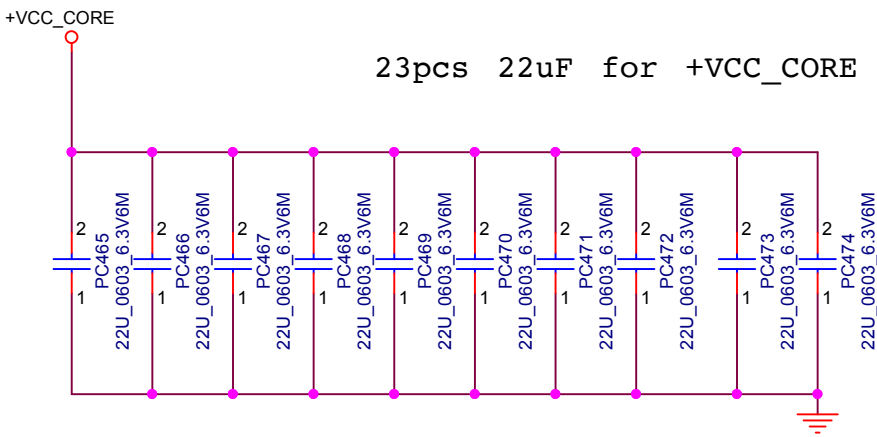


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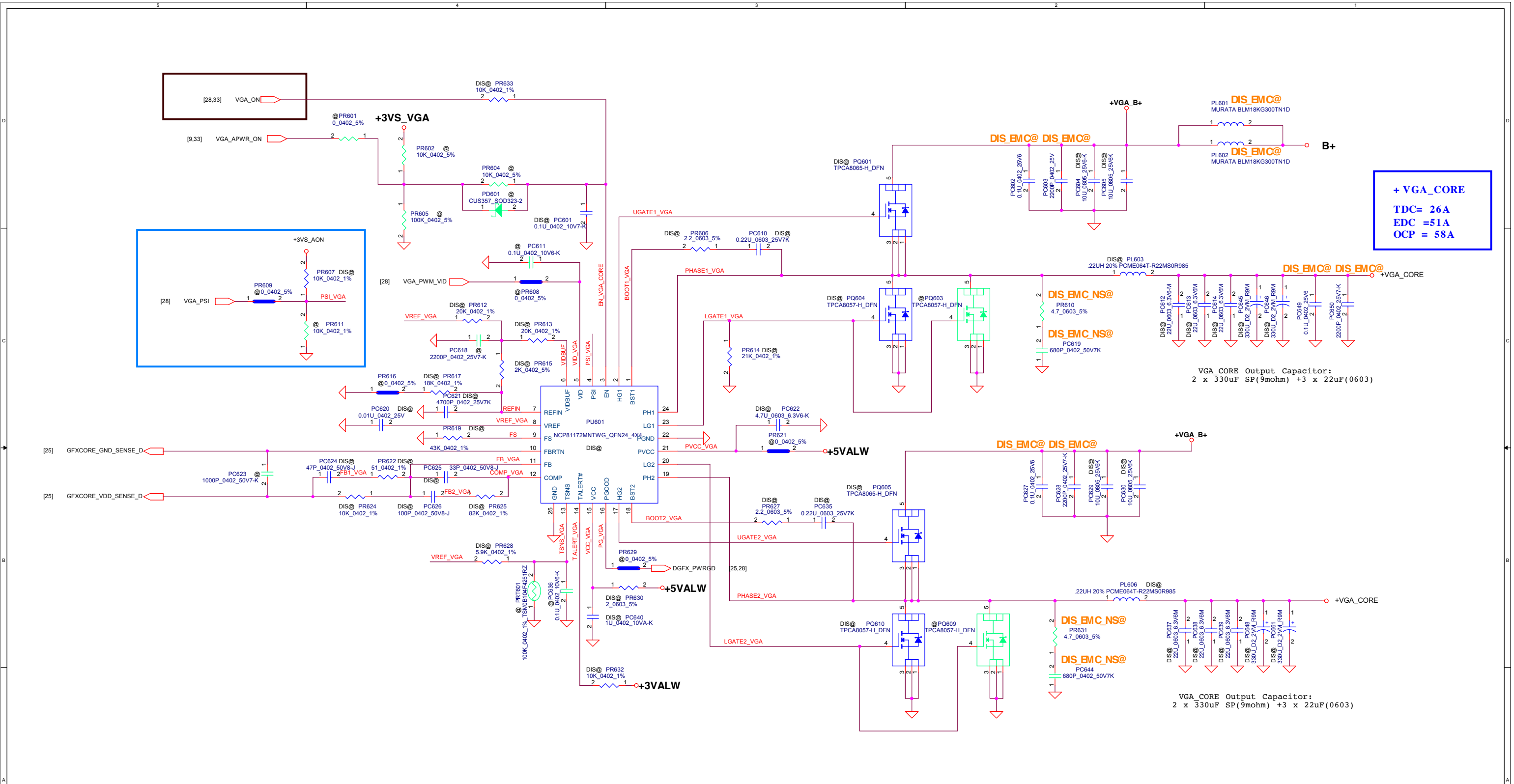


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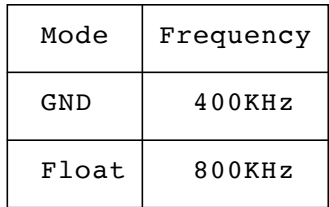
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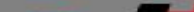


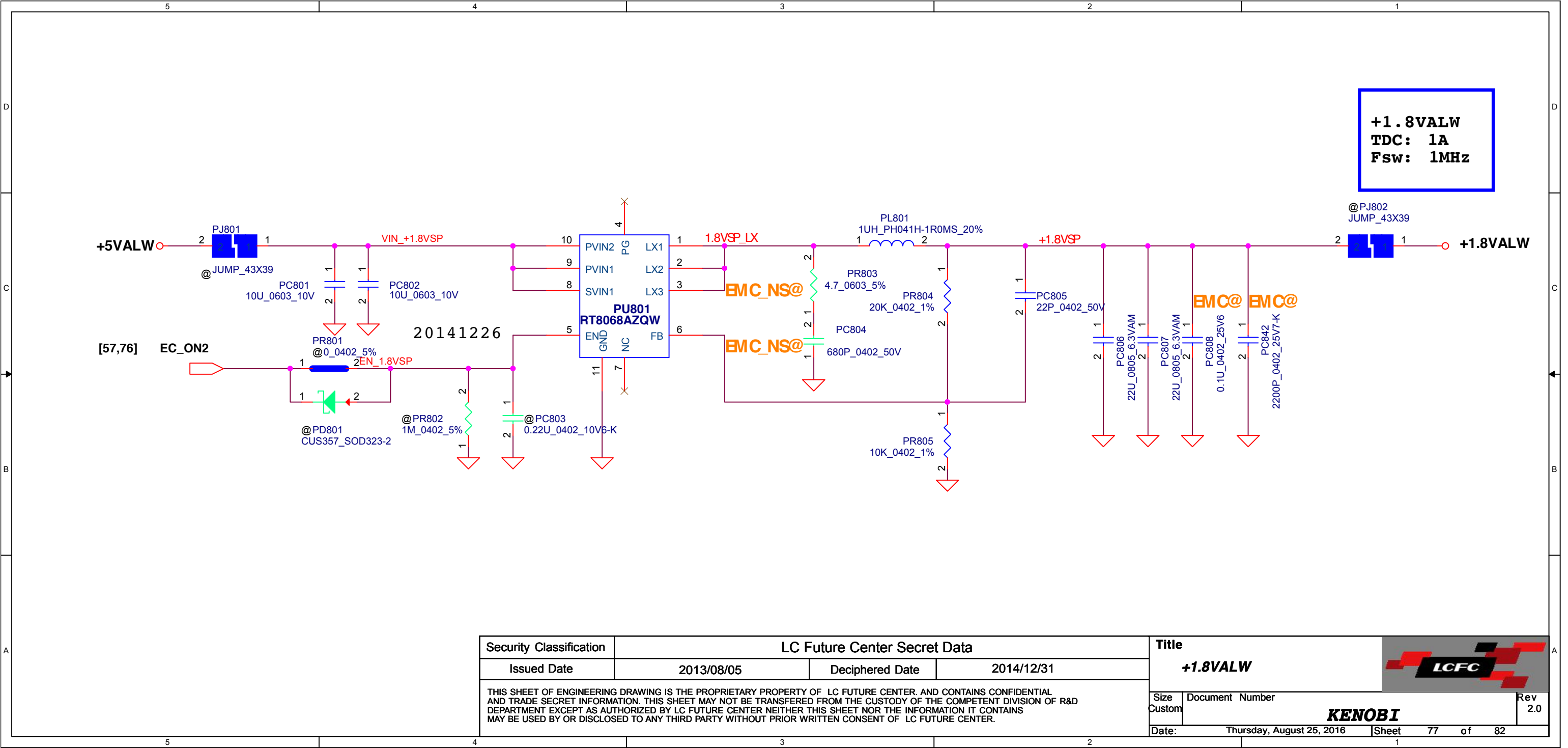
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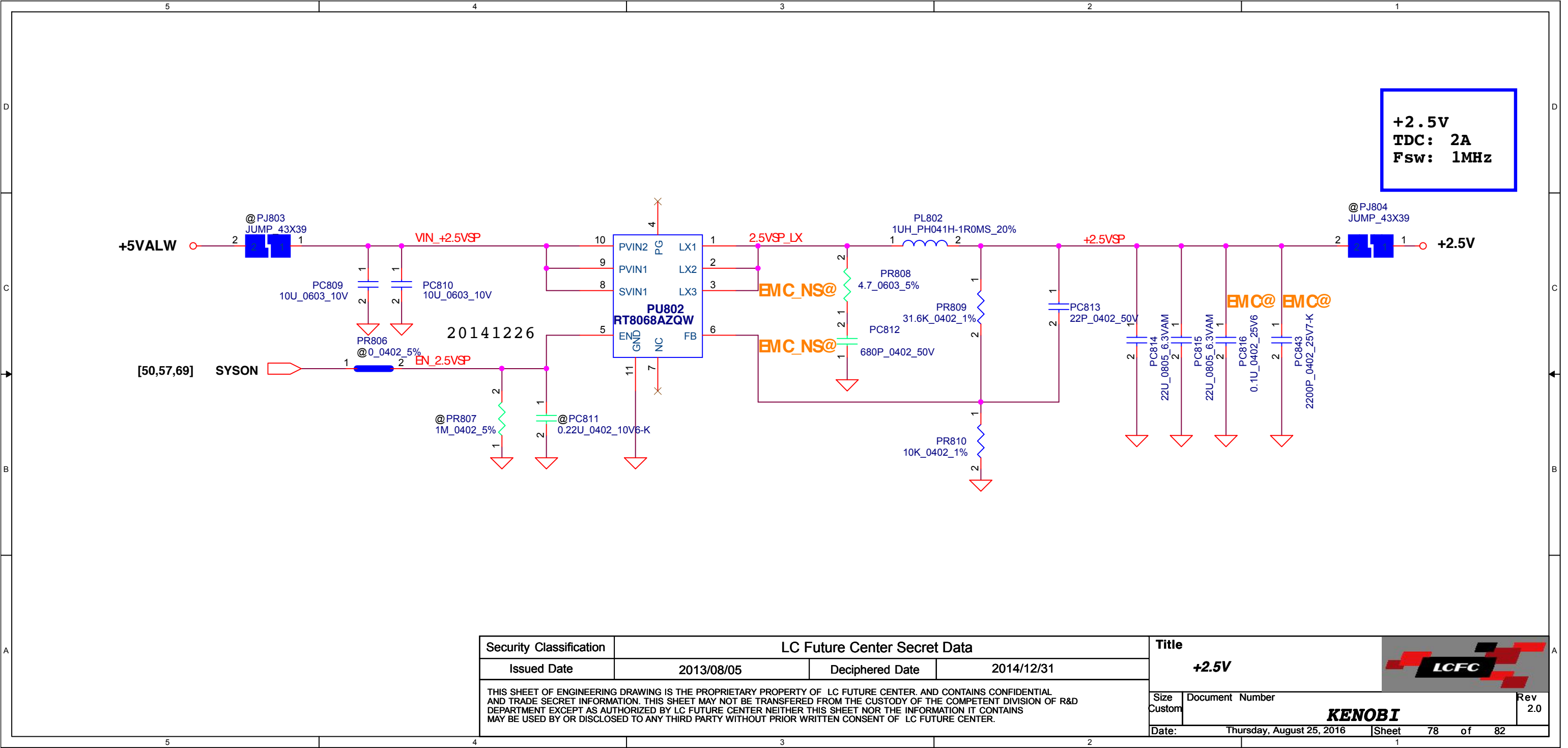


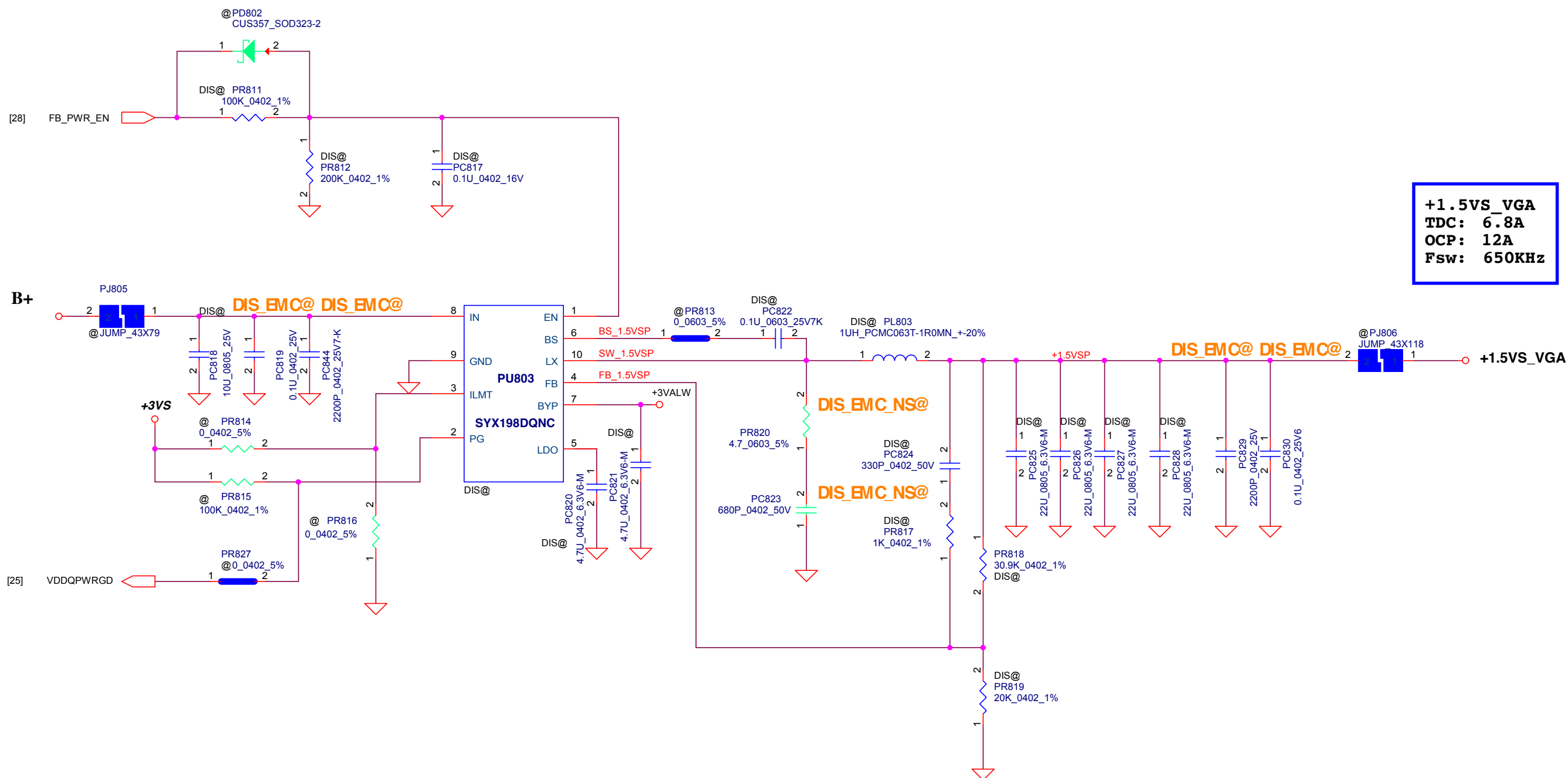
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Date: Thursday, August 25, 2016				Sheet	76 of 82	

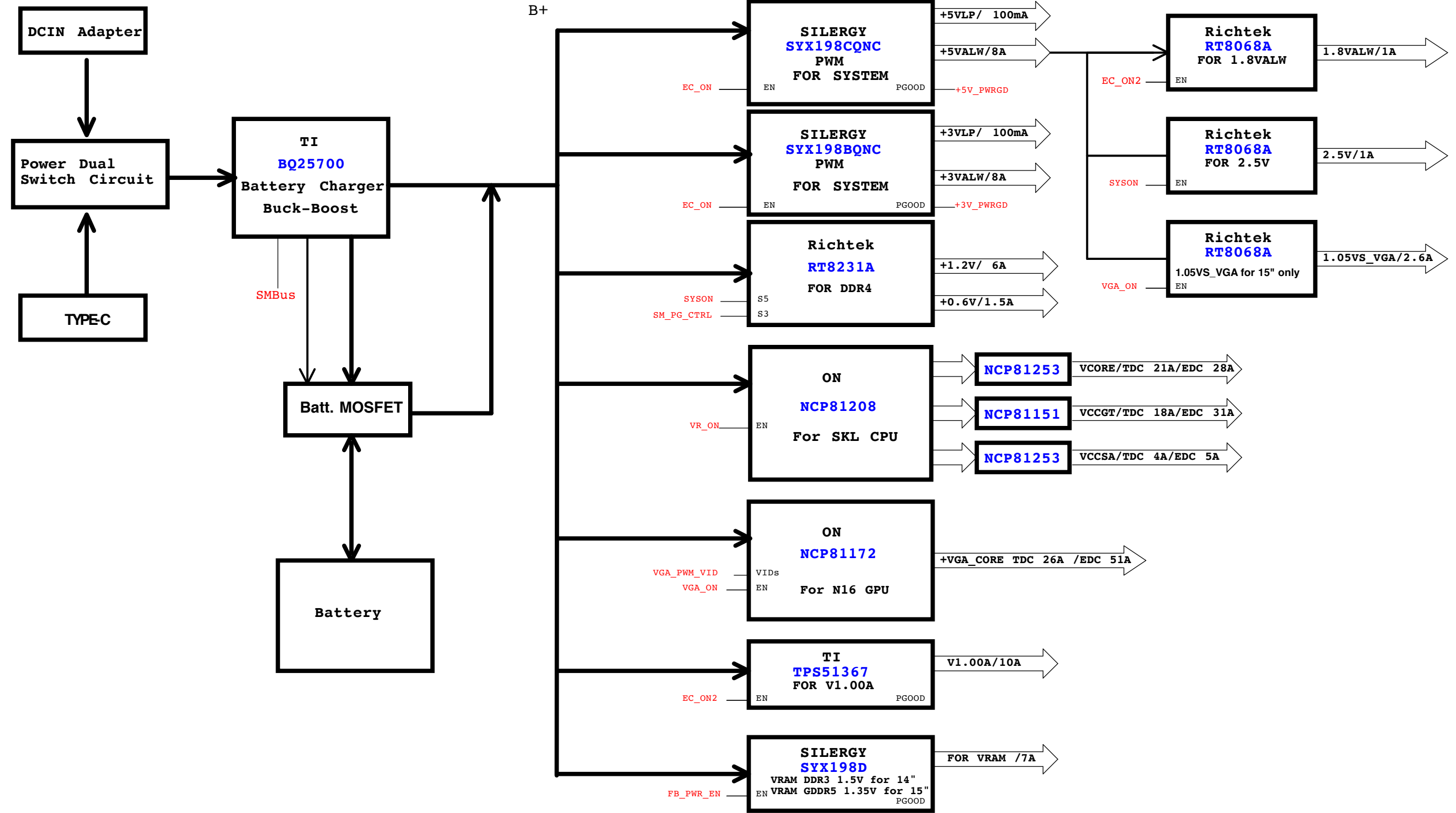






+1.5VS_VGA
TDC: 6.8A
OCP: 12A
Fsw: 650KHz

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The central portion of the image is a large, empty white rectangle, which serves as the workspace for the engineering drawing.

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The central portion of the image is a large, empty white rectangle, which serves as the workspace for the engineering drawing.